

Integration of a Pilot-Tone Based BPM System within the Global Orbit Feedback Environment of Elettra

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In this contribution, we describe the advantages of the pilot tone compensation technique that we implemented in a new BPM prototype for Elettra 2.0. Injecting a fixed reference tone upstream of cables allows for a continuous calibration of the system, compensating the different behaviour of every channel due to thermal drifts, variations of cable properties, mismatches and tolerances of components.

The system ran successfully as a drop-in substitute for a Libera Electron not only during various machine shifts, but also during a user dedicated beamtime shift for more than 10 hours, behaving in a transparent way for all the control systems and users. The equivalent RMS noise (at 10 kHz data rate) for the pilot tone position was less than 200 nm on a 19 mm vacuum chamber radius, with a long-term stability better than 1 μ m in a 12-hour window.

Two main steps led to this important result: firstly, the development of a novel RF front end that adds the pilot tone to the signals originated by the beam, secondly, the realisation of an FPGA-based double digital receiver that demodulates both beam and pilot amplitudes, calculating the compensated X and Y positions.

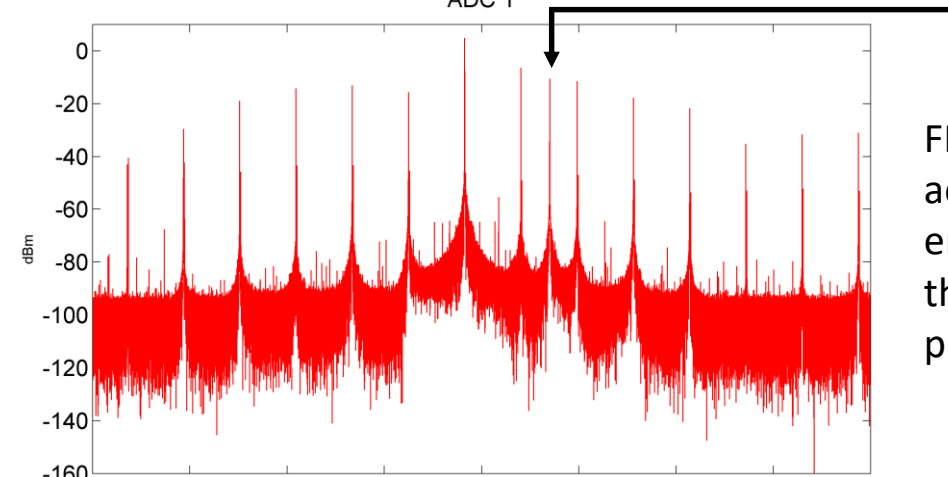
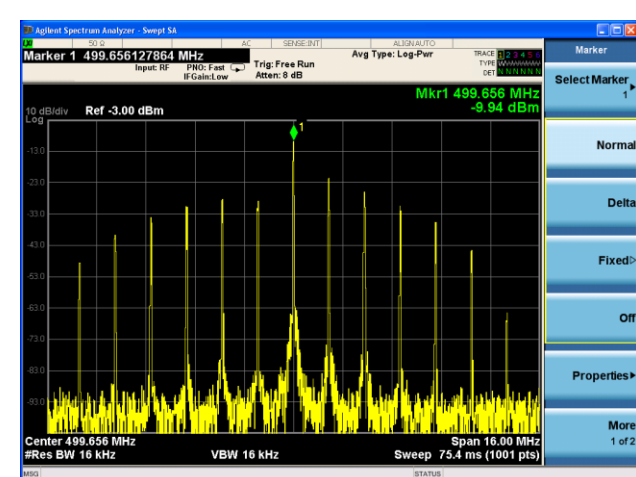
Proposed compensation

$$A(f) \xrightarrow{P(f)} A_P(f) + A_M(f) \quad A_P(f) = H_A(f) \cdot P(f) \quad A_M(f) = H_A(f) \cdot A(f) \quad A(f) = \frac{A_M(f)}{A_P(f)} \cdot P(f)$$

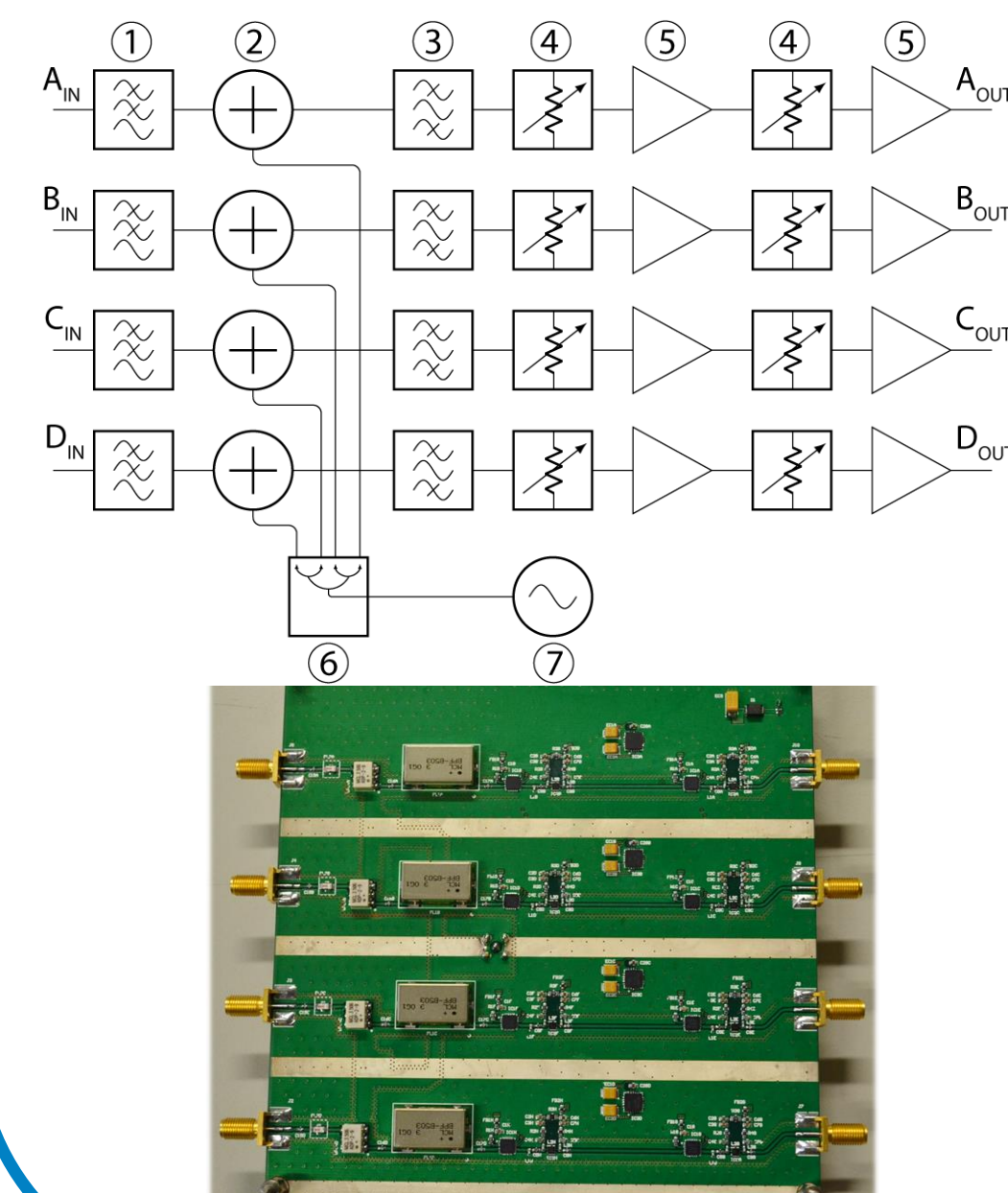
$$x = K_x \cdot \frac{A_M/A_P - B_M/B_P - C_M/C_P + D_M/D_P}{A_M/A_P + B_M/B_P + C_M/C_P + D_M/D_P}$$

The DoS algorithm is sensitive to inter-channel gain differences, in particular if these are time-variant. The proposed compensation adds a fixed sinusoidal tone (same for all the channels) to the original signal. In order to achieve an effective correction, the pilot-tone frequency has to fall near the carrier one, without interfering with the latter. The equations above show the model used: $A(f)$ is the input signal, $P(f)$ the reference tone, $H(f)$ the response of the channel (all in frequency domain). The position of the tone is crucial: only the gaps between the harmonics (spaced by the revolution frequency, 1.156 MHz) are suitable frequencies.

Spectrum of the signal coming directly from the electrodes



Analog RF front end

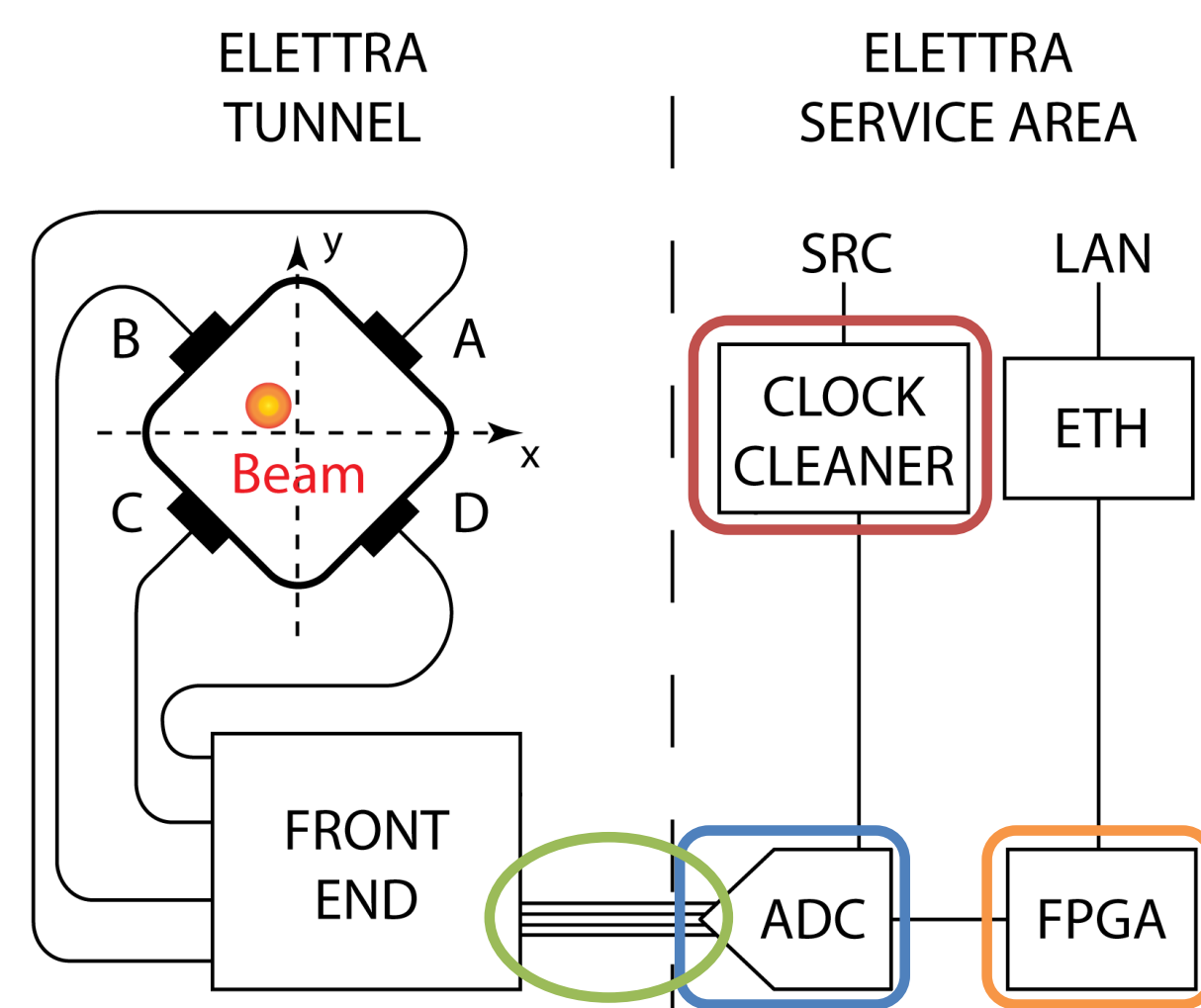


Figures on the left show the block diagram of the system and the manufactured board:

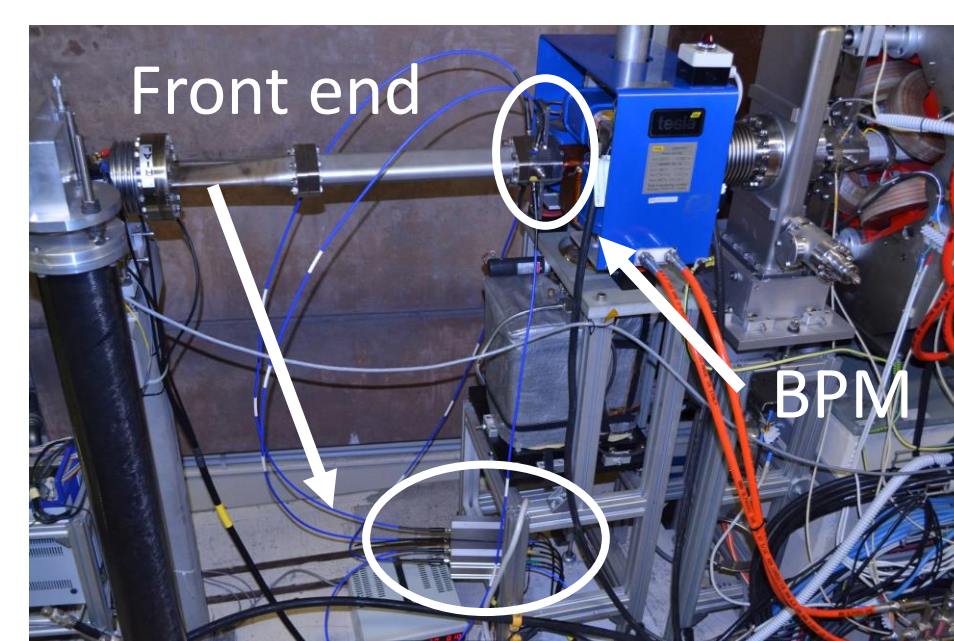
- the internally generated (by a PLL) pilot tone is split into four paths by a high-reverse-isolation splitter that guarantees more than 52 dB of separation between the outputs;
- a coupler sums the tone with the signal from the pick-ups, adding further 25 dB of isolation to prevent inter-channel crosstalk from the path of the pilot tone;
- all the signals pass through a bandpass filter, centered at 500 MHz with a bandwidth of 15 MHz, and two variable-gain stages, composed of low-noise, high-linearity amplifiers ($G=22$ dB, $F=0.5$ dB) and digitally controlled attenuators (up to 31.75 dB of attenuation, steps of 0.25 dB).

It has to be noted that being the front end a separate unit, it can be placed as near as possible to the pick-ups, with two main advantages: better signal-to-noise ratio and the possibility to compensate the cables.

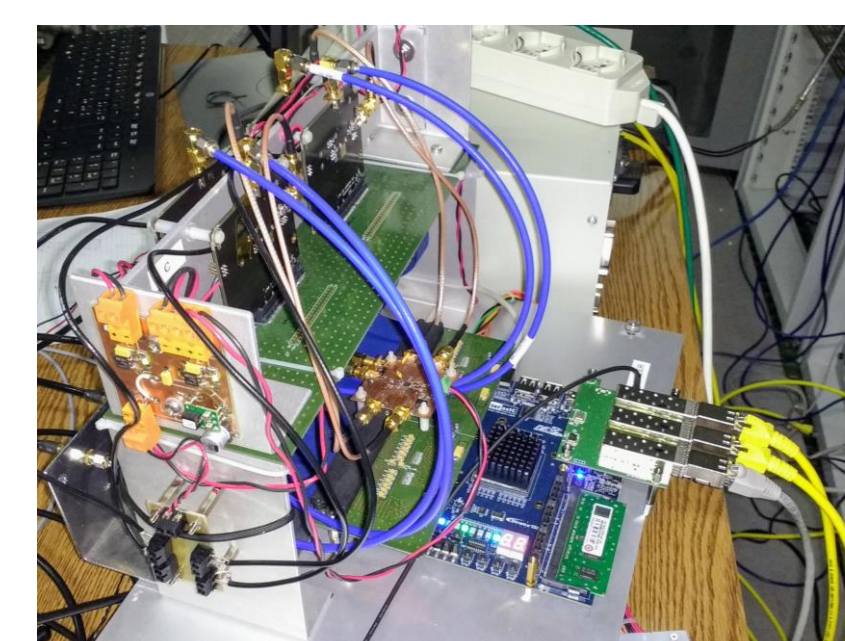
Measurement setup



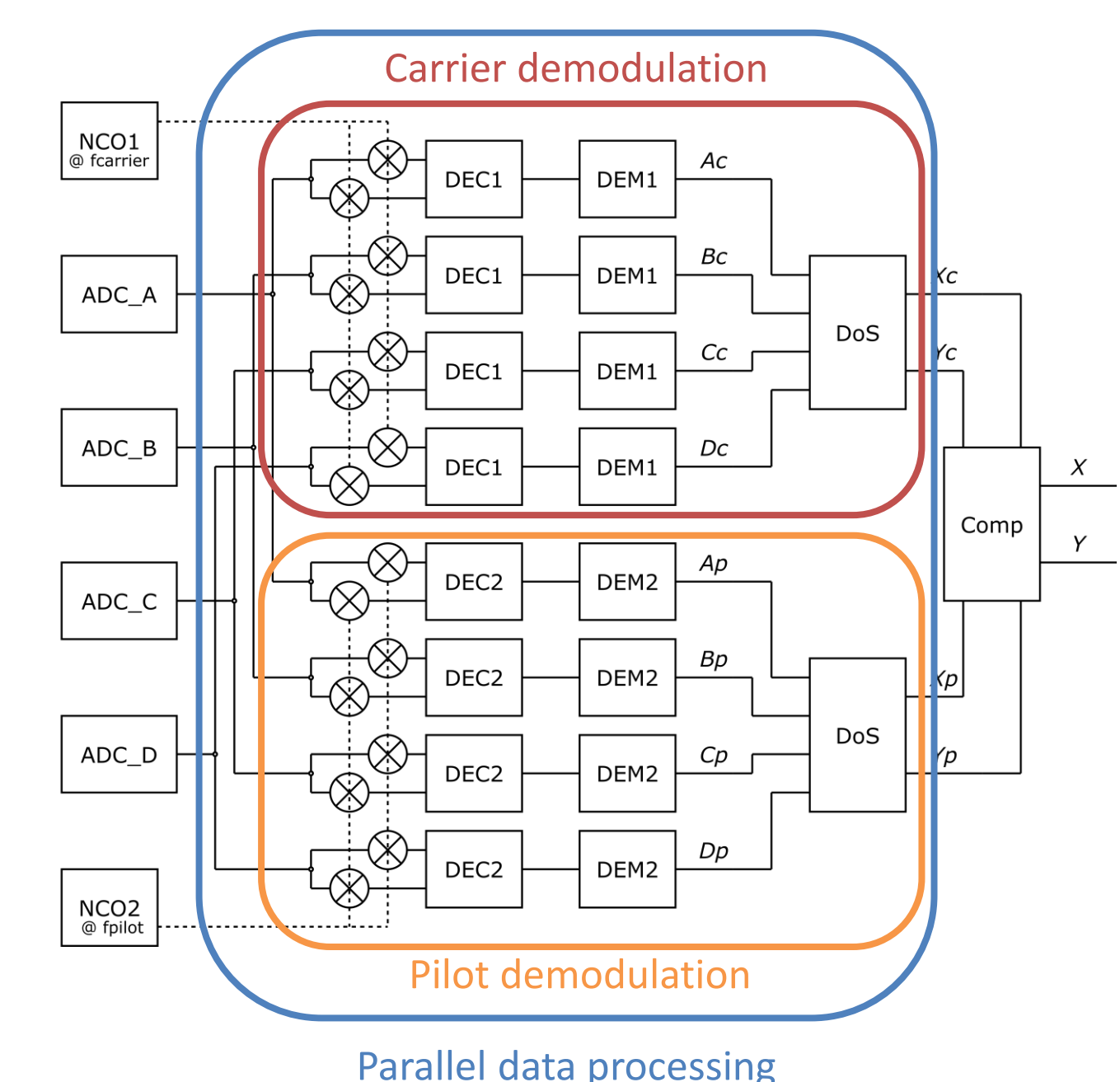
The following results have been collected with Elettra storage ring running in normal operation, 2.0 GeV and 310 mA. The BPM pick-ups used are close to an insertion device and between two bellows. The bellows assure the mechanical decoupling from the rest of the machine. The beam orbit is kept stable at the center position by the global feedback.



The RF front end has been placed in Elettra tunnel area and connected to a button BPM of the storage ring (chamber average radius ~ 19 mm), allowing the compensation of cables. The in-house assembled digitiser is located in the service area.



The digitiser demodulates in a parallel and continuous way both the carrier and the pilot inside the FPGA. The compensated data at 10 kHz is sent through a Gigabit Ethernet connection to the Global Orbit Feedback system.

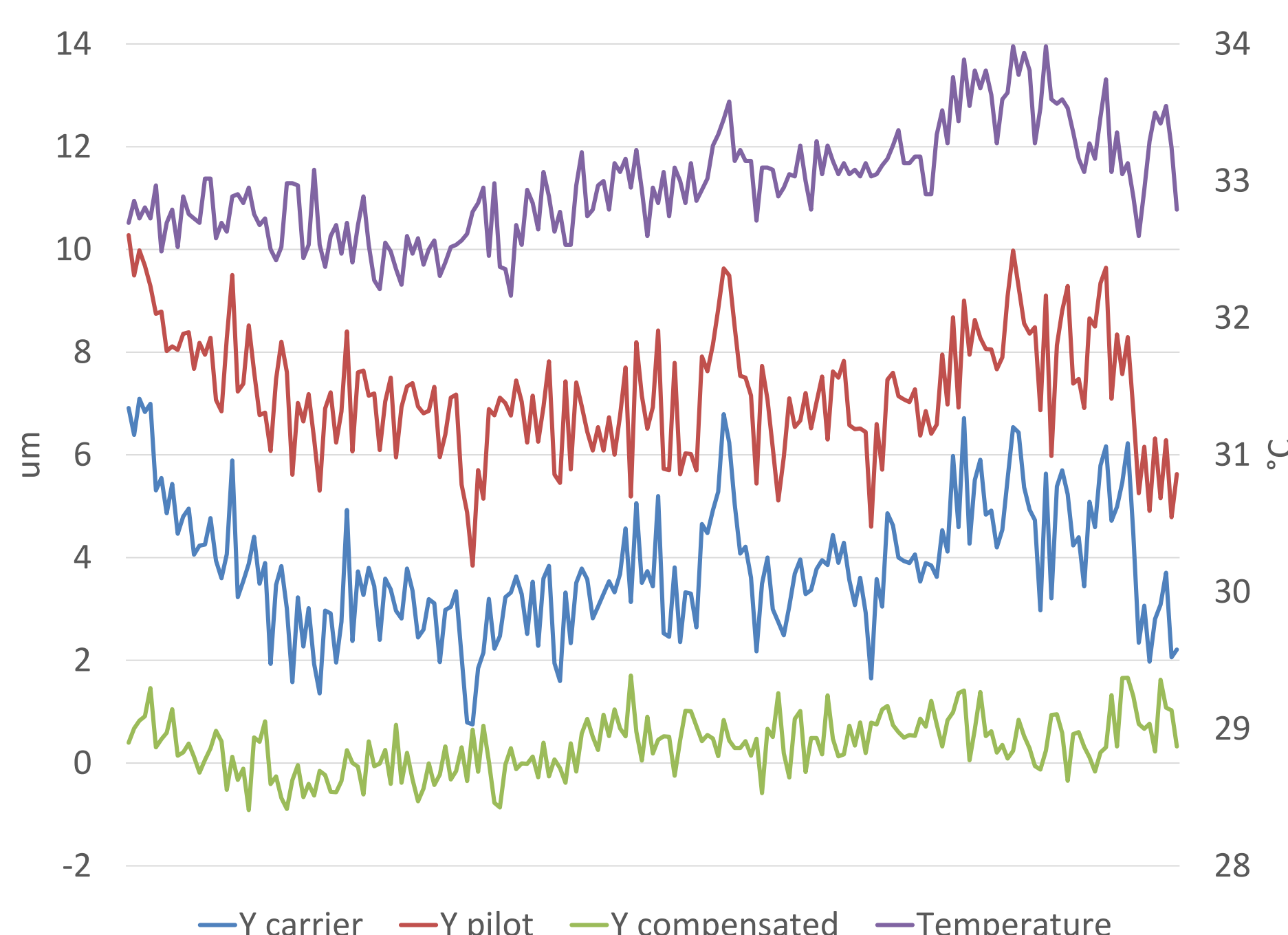


Results

- The 499.654 MHz carrier and the 502.051 MHz pilot tone are undersampled respectively at 19.654 MHz and 22.051 MHz.
- The input signal coming from the beam is about -6 dBm with 310 mA of current.
- All the FPGA processing clocks are in phase with Elettra machine clock.
- Carrier and pilot amplitudes measured at the ADCs input are both 0 dBm, for a total amplitude of +6 dBm, that corresponds at the 80% of the ADCs working range.

- Resolution in real conditions (front end + cables): ~ 180 nm @ 10 kHz with $K=19$ mm
- Resolution with an RF generator directly at ADCs input: ~ 50 nm @ 10 kHz with $K=19$ mm
- Influence of the pilot on the calculated position: no changes have been seen switching on and off the tone.
- Long-term stability better than 1 μ m in 24 hours.
- The pilot position returns a diagnostic of the system status, so hardware faults can be identified.

Changes in temperature and positions



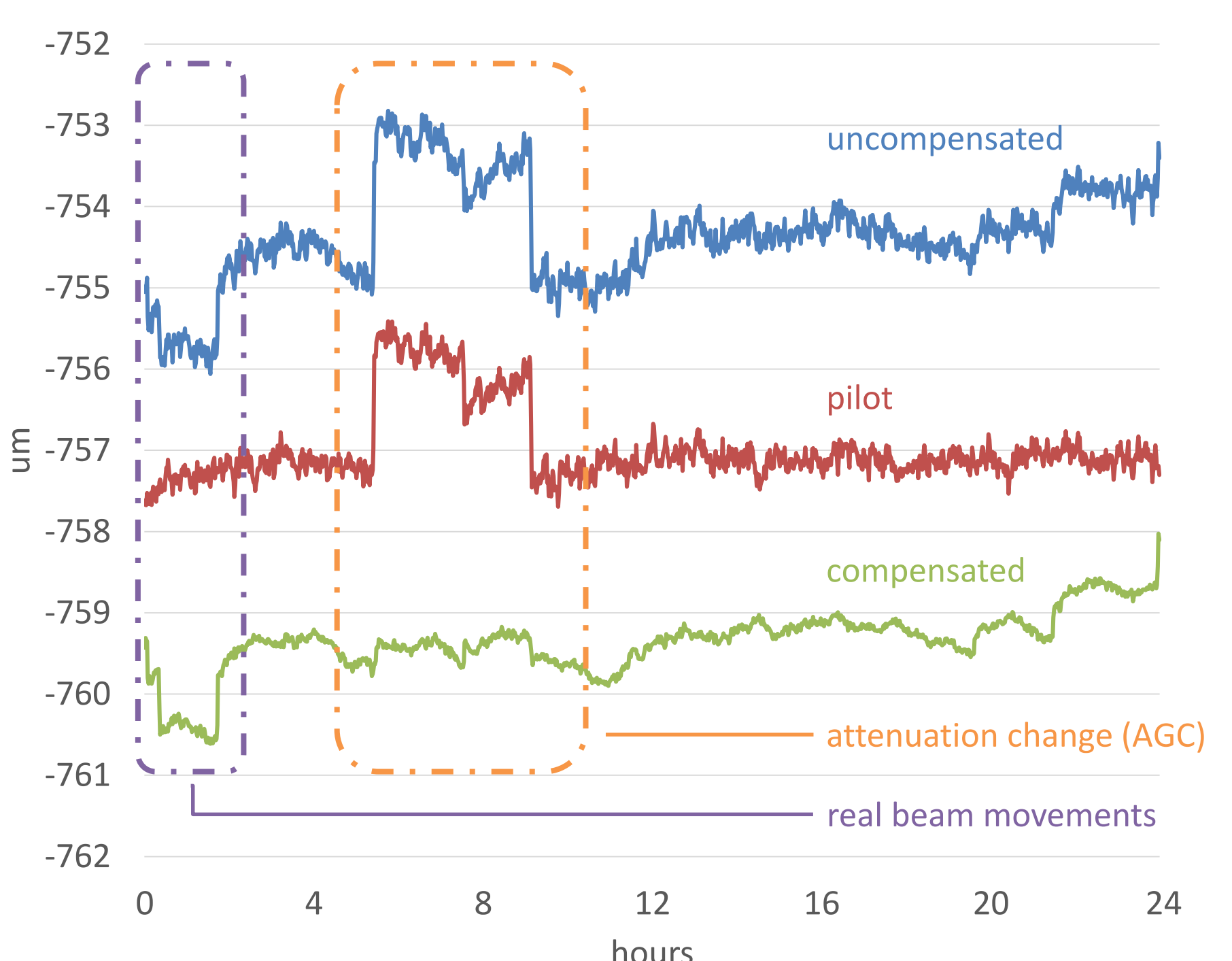
The figure on the left shows dependence of the calculated position on the temperature of the ADCs (measured with sensors).

- A real signal from the beam emulates a centered and stable beam (using a splitter).
- Identical thermal drifts affect the carrier and the pilot.
- The compensation improves the standard deviation of the position from 1.26 μ m to 0.54 μ m in a time window of 24 hours.

The figure on the right shows how compensation can be useful for long-term stability.

- The correction reduces the standard deviation by a factor of two, from 0.63 μ m to 0.38 μ m.
- The average considered radius of the chamber is always 19 mm.
- The position is calculated on real signals from the beam, without using a splitter.
- The jump in Y-position due to attenuation change is greatly reduced using the compensation.

Beam Y-position in a 24-hours time window



REFERENCES

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FUTURE WORK

- Optimization of the characteristics of the pilot tone (amplitude, frequency) in relation to the compensation
- Development of a FMC digitizer board with new 16-bit, 210 MS/s ADCs
- Hardware improvement in the front end: evaluating various filters for single pass machines