



The GBT-based Expandable Front-End (GEFE)

(A new radiation tolerant acquisition system for beam instrumentation)

The GEFE team: M. Barros Marin, A. Boccardi, C. Donat Godichal, J.L. Gonzalez, T. Lefevre, T. Levens & B. Szuk



Knowledge Transfer
Accelerating Innovation

1. Abstract

The Giga Bit Transceiver based Expandable Front-End (GEFE) is a multipurpose FPGA-based radiation tolerant card, produced under the CERN Open Hardware License (CERN DHL). It is foreseen to be the new standard FMC carrier for digital front-end applications in the CERN BE-BI group. Its intended use ranges from fast data acquisition systems to slow control installed close to the beamlines, in a radioactive environment exposed to total ionizing doses of up to 75 krad (750 Gy). This poster introduces the architecture of the GEFE, its features as well as examples of its application in different setups.

2. The GEFE

General purpose FPGA-based **radiation tolerant(2.1)** board

Optical & Electrical interfaces (2.2):

- GBT-Versatile Link from CERN PH-ESE
- Custom Electrical Serial Link Transceiver (ESLT)

Upgradable (2.3):

- FPGA Mezzanine Card (FMC) High-Pin Count (HPC) connector
- 2x **GPIO connectors** (24 & 13 user I/Os respectively)

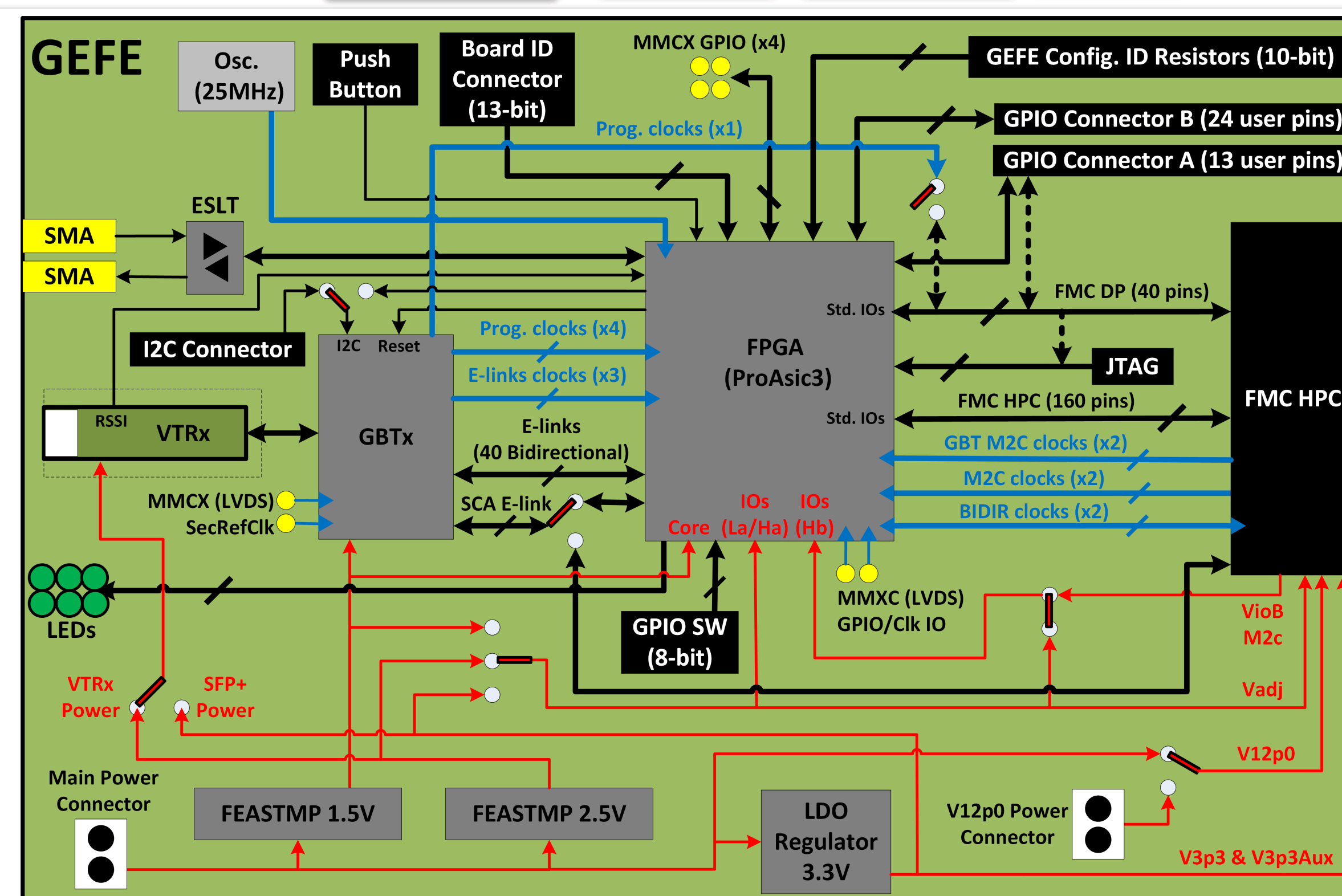
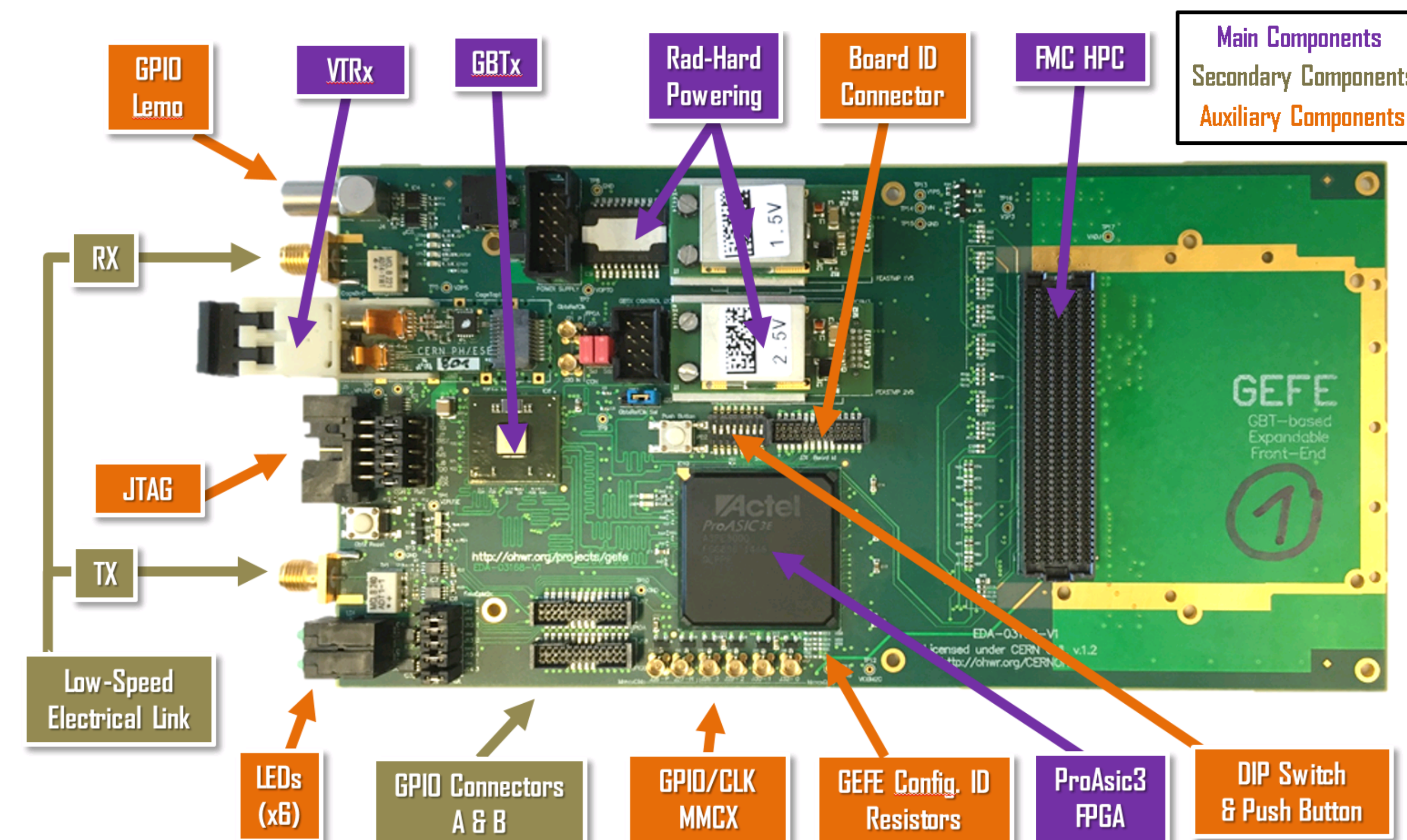
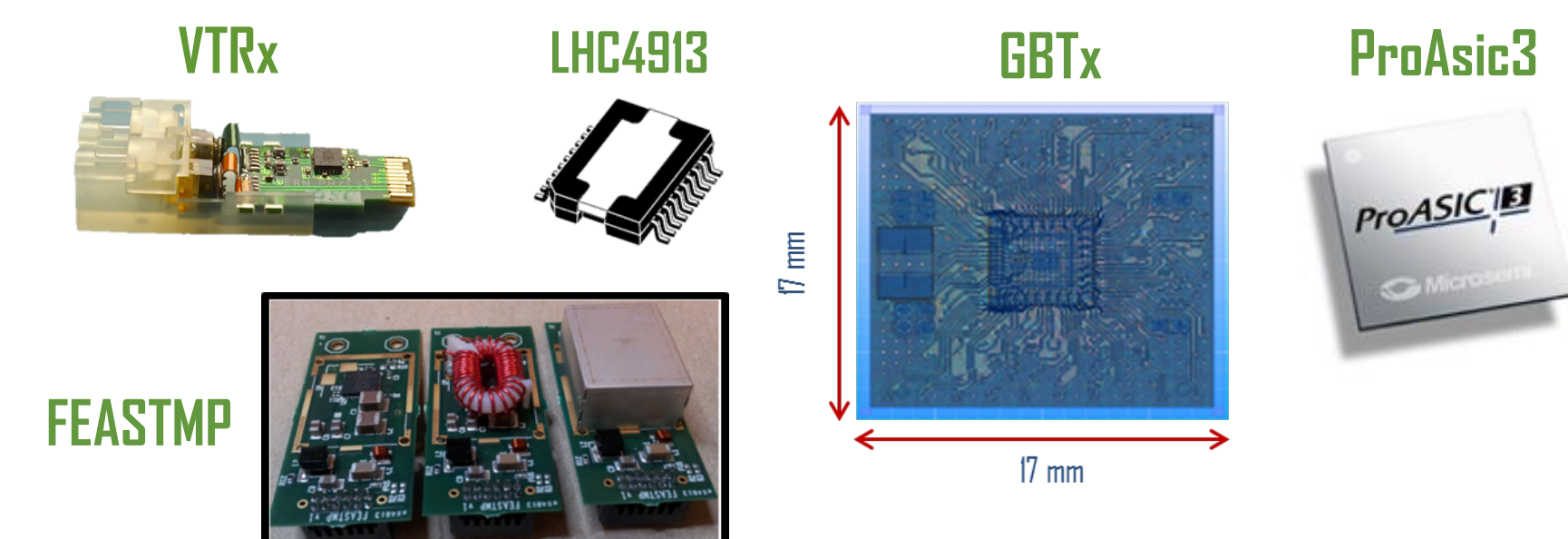
Flexible (2.4):

- FPGA **ProAsic3** (ACLA3PE3000-FGG896) from Microsemi
- Clocks, Resets, FPGA programming, Slow Control (SC) E-link & Power

2.1 Radiation Tolerant

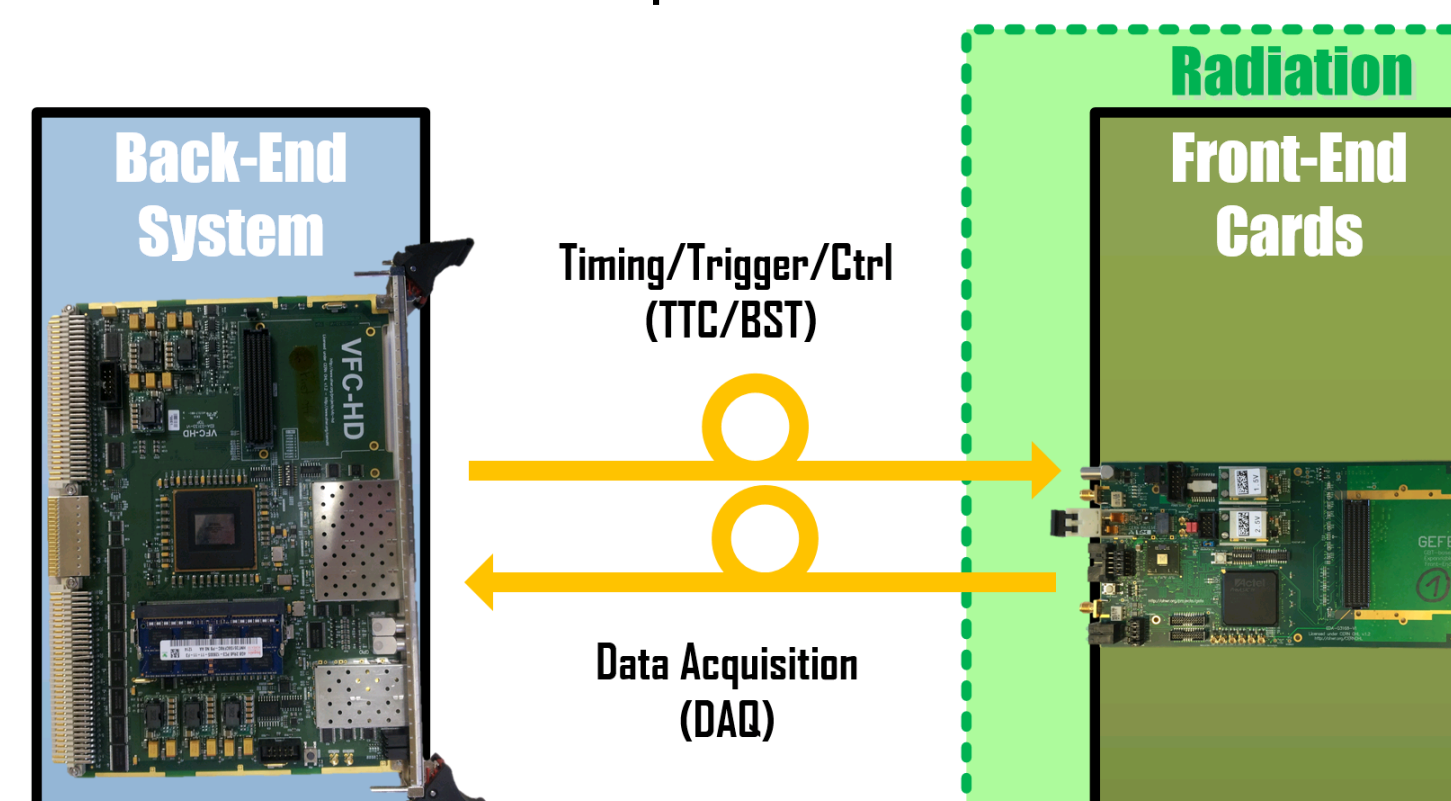
Target Total Ionizing Dose (TID): up to 75 krad

Active Component	Description	Manufacturer	Rad-hard by design	Max. TID
VTRx	Optical Transceiver	CERN PH-ESE	YES	up to 5 MGy
GBTx	Multi Gigabit Transceiver	CERN PH-ESE	YES	up to 1 MGy
FPGA (ProAsic3)	A3PE3000-FGG896	Microsemi	NO	up to 750 Gy
FEASTMP	DC/DC Regulator	CERN PH-ESE	YES	up to 2 MGy
LHC4913	LDO Regulator	ST Microelectronics	YES	up to 5 kGy
SN74V027450DCT	Dual Bit-Dual-Supply Bus Transceiver	Texas Instruments	NO	above 750 Gy
M65PND22T16	N-CHANNEL MOSFET with Diode	ON Semiconductor	NO	above 750 Gy
SN65LVDS2DBVR	High-Speed Differential Line Receiver	Texas Instruments	NO	above 750 Gy
SPX0010077	Crystal Oscillator (25MHz)	IQD Frequency Products	NO	above 750 Gy
BAV99	High Speed Switching Diode	FAIRCHILD/MULTICOMP	NO	above 750 Gy



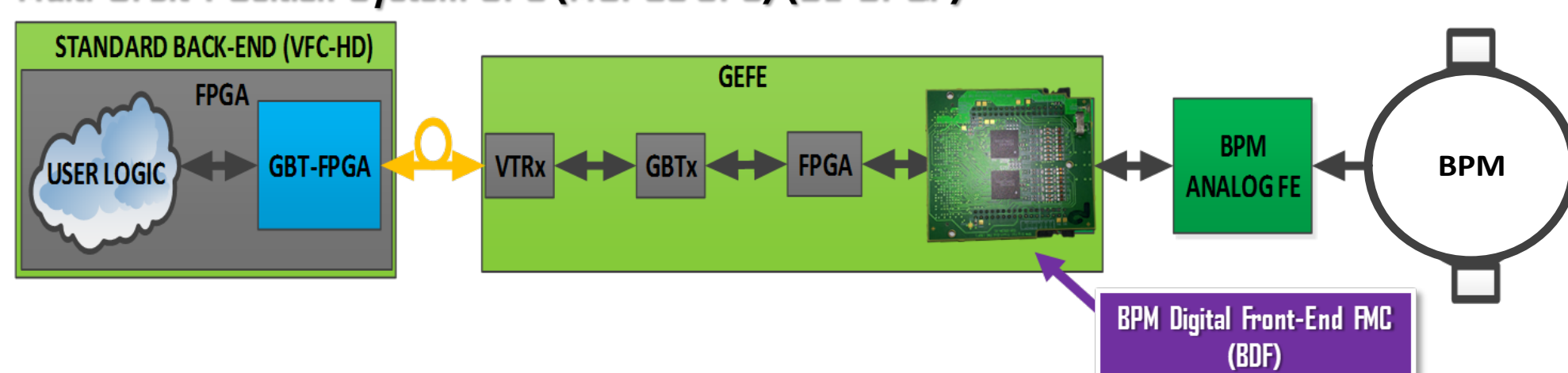
2.2 Optical & Electrical Interfaces

The GEFE takes advantage of the **Giga Bit Transceiver (GBT)/Versatile Link** platform developed by the CERN PH-ESE group. This provides a radiation hard, high-speed (4.8 Gbps), bidirectional, optical link for communication with back-end electronics, and multiple low-speed (40@80 MHz, 20@160 MHz or 10@320 MHz) electrical links (e-links) for communication with digital front-end electronics. The link can be fixed and deterministic in clock phase and data latency if required. In addition to the high-speed optical link, the GEFE features a **custom Electrical Serial Link Transceiver** to be used in low-speed communications over copper cable through long distances (tested up to 2 km@10 Mbps). The variety of optical and electrical interfaces on the board, in addition to its flexible architecture, mean that it can easily be adapted for use in many different applications where radiation tolerance is a requirement.

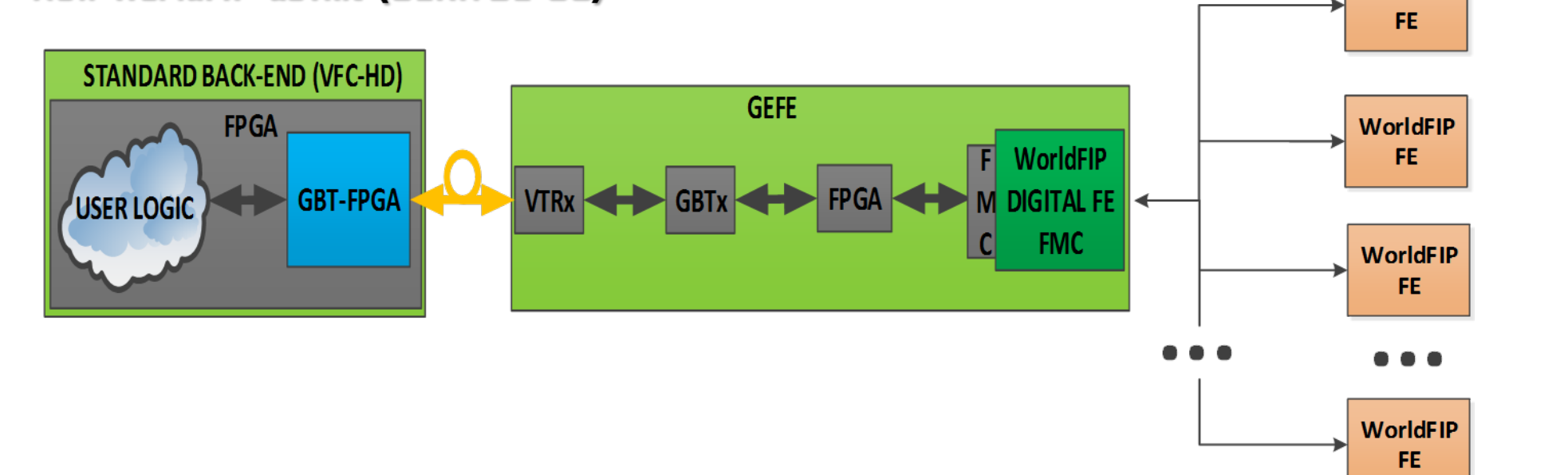


3. Application Examples

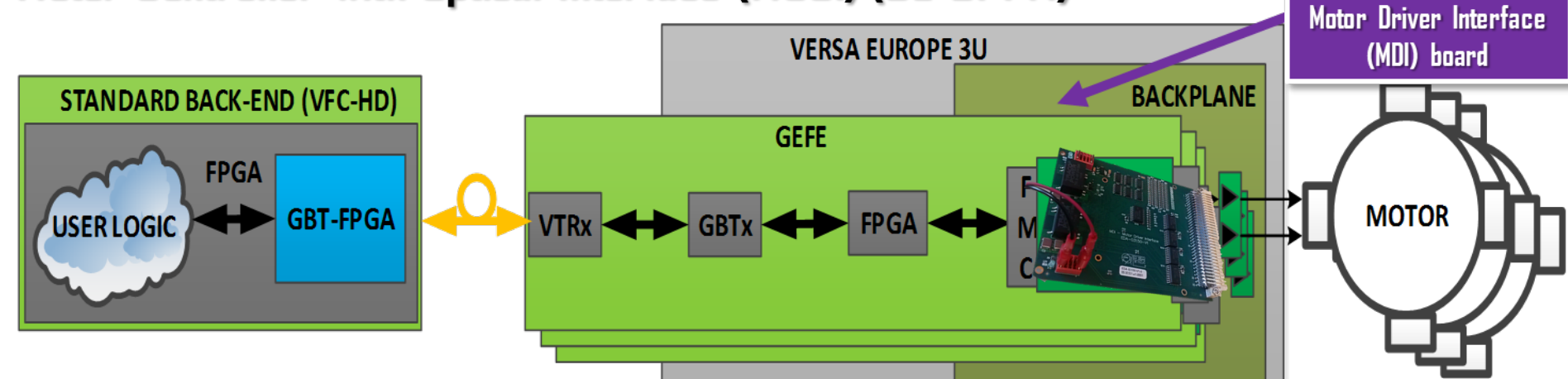
Multi-Orbit Position System SPS (MOPPS SPS) (BE-BI-DP)



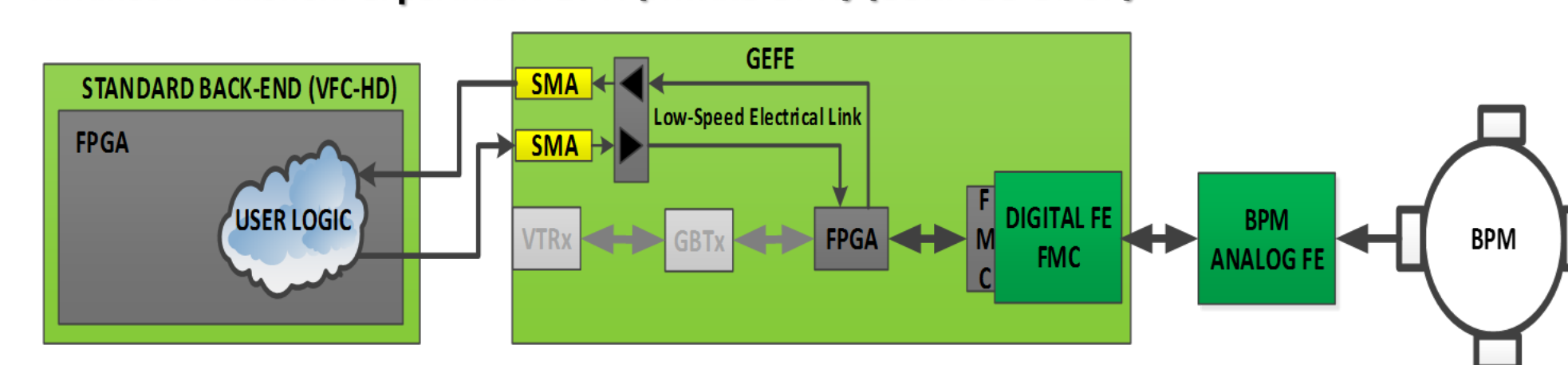
New WorldFIP devkit (CERN BE-CD)



Motor Controller with Optical Interface (MCOI) (BE-BI-PM)



Advanced Wakefield Experiment BPM (AWAKE BPM) (CERN BE-BI-DP)



2.4 Flexible

The interface between the e-links and the digital front-end electronics plugged onto the different on-board connectors as well as the control of the different on-board resources (e.g. LEDs, etc.) is carried out by a **Microsemi ProAsic3 flash-based FPGA**, device that has been qualified for operating in radiation environments. All other components are also (or will be) qualified for use in environments with high levels of radiation. The use of an FPGA, coupled with flexible powering, clocking and FPGA programming schemes, provides the capability to adapt the GEFE for interfacing to the user's systems.



ProASIC3E	A3PE3000
System Gates	3,000,000
Equivalent LEs	35K
VersaTiles (D-Flip-Flop)	75,264
RAM kbits (1,024 bits)	504
4,608-Bit Blocks	112
FlashROM Bits	1,024
Secure (AES) ISP ²	Yes
Integrated PLLs in CCCs ³	6
VersaNet Globals	18
I/O Standards	Pro
I/O Banks (~JTAG)	8
Maximum User I/Os	620
Typical Static / Flash-Freeze Power (mW) at V _{CC} =1.2 V	3.30
Single-Ended I/Os / Differential I/O Pairs	620/310

2.3 Upgradable

In order to maximize the versatility, the GEFE is expanded with dedicated front-end cards through a **High-Pin Count FPGA Mezzanine Card (FMC HPC) connector** which features up to 160 user-specific I/Os (that can be configured both as single-ended or differential pairs) as well as 4 differential clock inputs and 2 differential bidirectional clocks. The high-speed lines (DP) of the FMC HPC connector are used as user-specific I/Os and can also be used for special functions (Please note that the use of the DP lines in GEFE does not comply with the FMC standard). In addition to the FMC HPC connector, the GEFE offers **2 general purpose connectors**. Both presenting the same form-factor (26-pin - .050" pitch).

4. Status & Outlook

The GEFE board

- Validity test of the first 2 prototypes of GEFE v1 (November 2015)
- Rad-Tolerance qualification of components (Second half of 2015) and full board (First half 2016)
- Pre-production stage (First half of 2016) (small orders for prototyping)
- Production stage (First half of 2017)

The GEFE community

- Open HardWare Repository (OHWR) Wiki and Email Lists
- 8 projects interested so far (New MOPPS SPS, CHARM test board, New Rad-Tolerant Fieldbus, etc.)
- About 350 pieces requested so far (36 already fabricated)
- Contact: manuel.barros.marin@cern.ch

Web site: <http://www.ohwr.org/projects/gefe>