Switched Mode Converters

(4 Quadrants)

Yves THUREL
CERN

4 Quadrant basic background

- 4Q. Conventions
- 4Q. Working area / loads
- 4Q. Basic schematics

4 Quadrant topologies Review

- Principle schematics (main ones presented)
- Advantages / Drawbacks
- Some realizations

4 Quadrant practical realization & example

- LHC Specifications
- LHC Topology choice explained
- LHC Converter principles
- Technical points highlighted (loops, circulating current,…)
- Realizations

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- **4Q. Basic schematics**

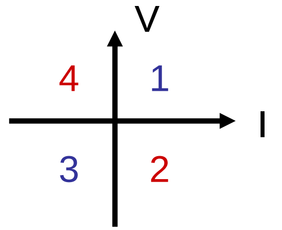
4 Quadrant topologies Review

- **Principle schematics (main ones presented)**
- **Advantages / Drawbacks**
- **Some realizations**

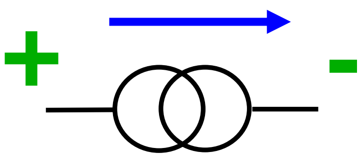
4 Quadrant practical realization & example

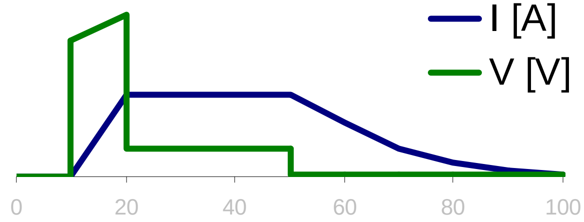
- **LHC Specifications**
- **LHC Topology choice explained**
- **LHC Converter principles**
- **Technical points highlighted (loops, circulating current,…)**
- **Realizations**

4 Quadrant Operation: Definition (applied to R-L circuit)



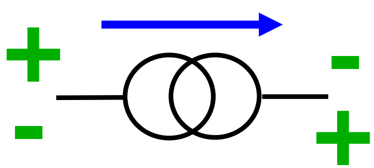
1 Quadrant mode

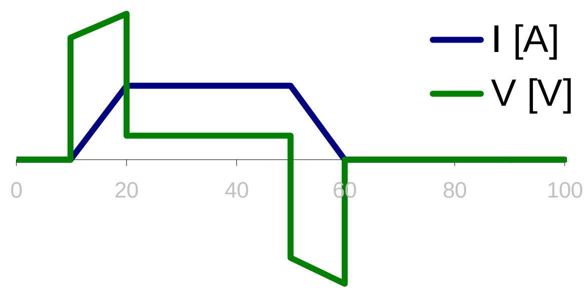




Control of the decreasing current is still possible within drastic conditions and limits. ($R_{CIRCUIT}$ acts as discharger.)

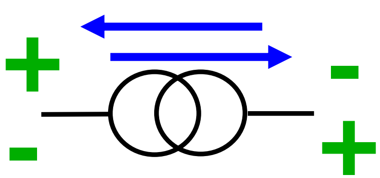
2 Quadrant mode

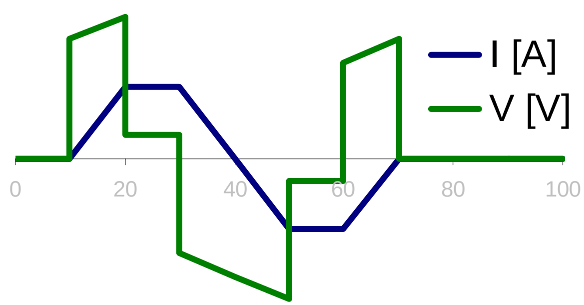




Current is controlled (being always in the same sense), when increasing or decreasing.

4 Quadrant mode

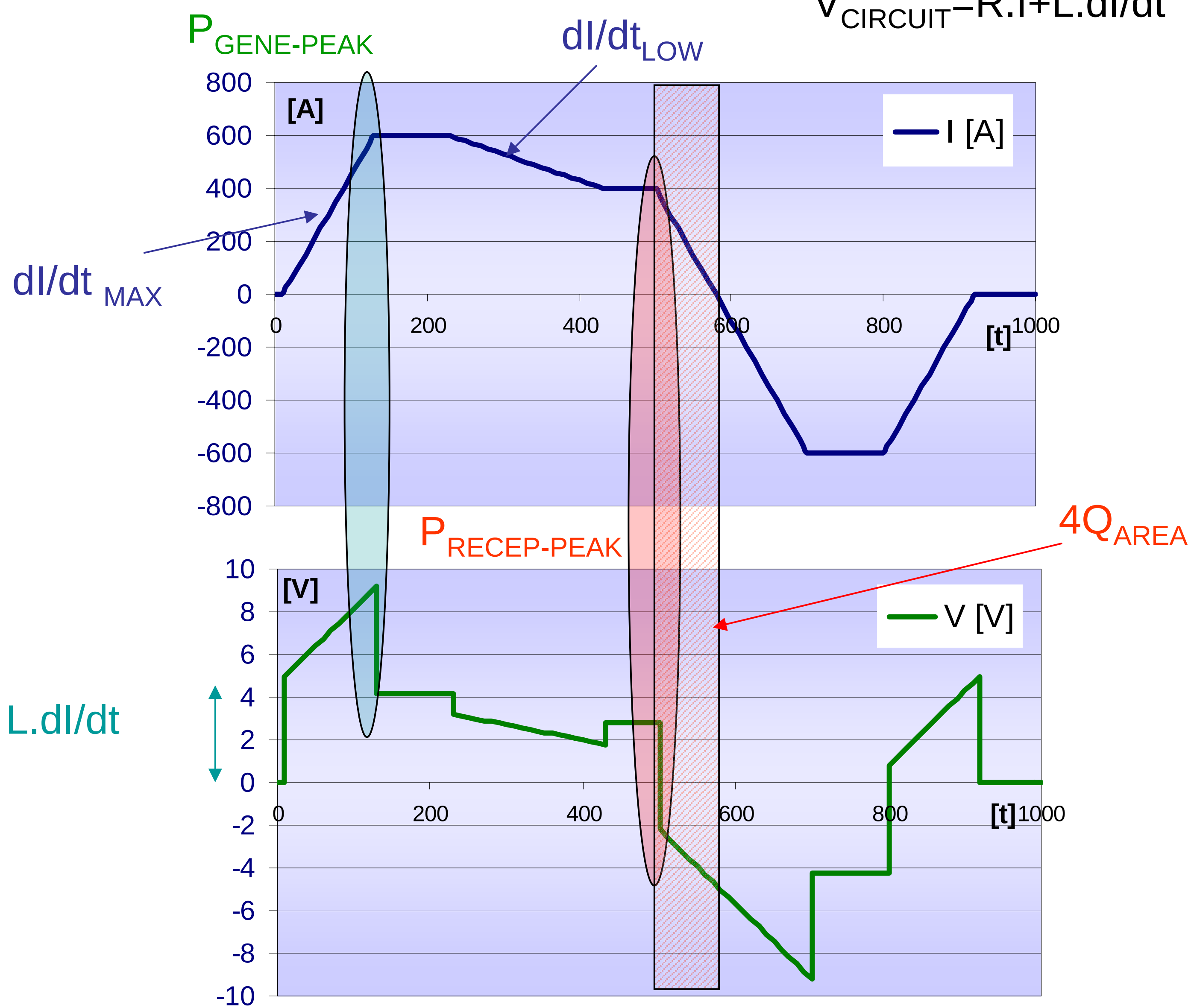




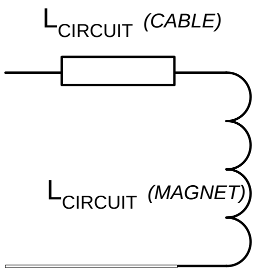
No theoretical operation limitation.

4 Quadrant Operation: Loads Typical Cycle (R-L)

$V_{CIRCUIT}=R.I+L.dI/dt$



CIRCUIT



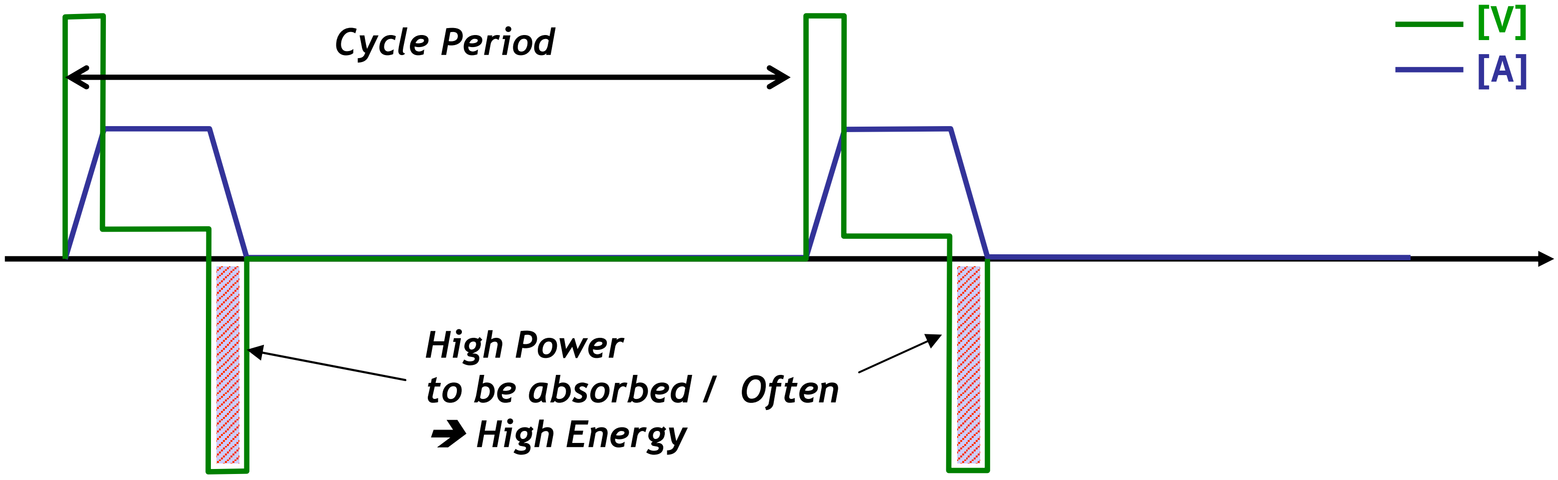
L = 1H
R = 7mOhms
$dI/dt_{MAX} = 5A.s^{-1}$
$I_{MAX} = 600A$

KEY FEATURES

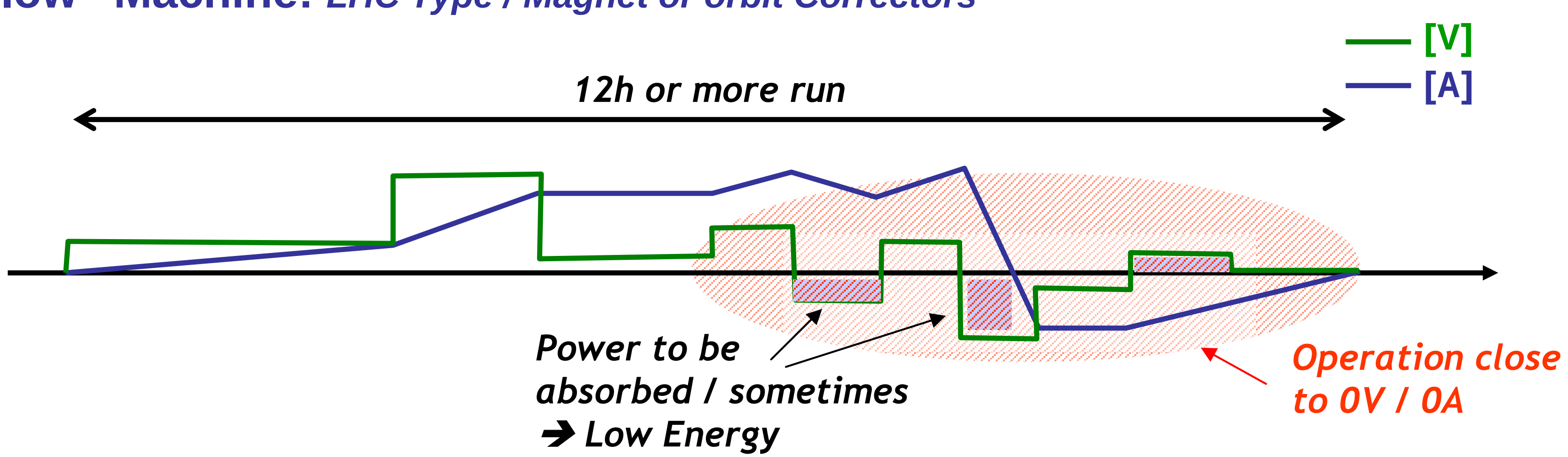
$L.dI/dt = 5V$
$R.I_{MAX} = 4.2V$
$V_{MAX} = 9.2V$

4 Quadrant Operation: Load Influence on topology

"Pulsed" Machine



"Slow" Machine: *LHC Type / Magnet or orbit Correctors*



4 Quadrant Operation: Load Impact on cost & design parameters

Circuit Characteristics

- L = 1H — *LHC Machine*
- dI/dt = 10A.s-1 — *LHC Machine*
- I = [-600A;+600A] — *LHC Machine*
- P_{Cable} < 15kW — *LHC Tunnel*

Circuit Key Features

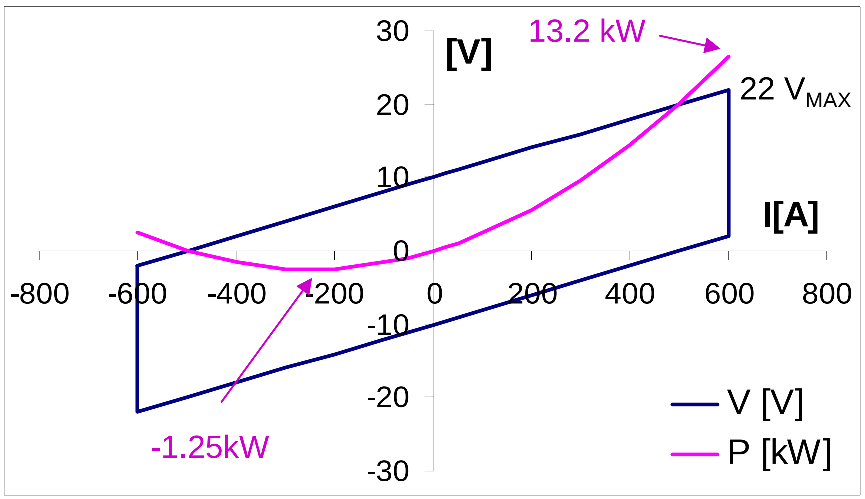
•L•di/dt = 10V

•10mOhms < R_{cable} < 21mOhms

6V < $R_{cable} \cdot I_{MAX}$ < 12V

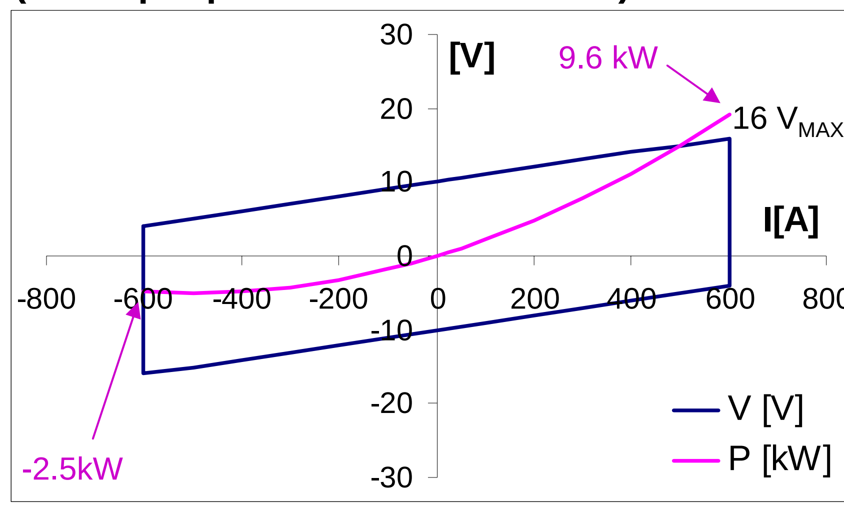
20 mOhms

(V: Output Voltage Power converter)



10 mOhms

(P: Output power Power converter)



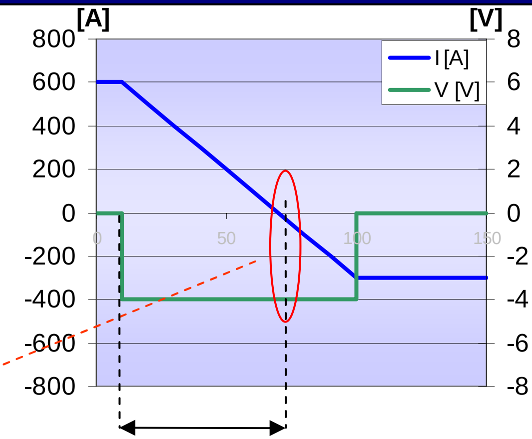
P_{MAX}	13.2kW	*100%*	P_{MAX}	9.6kW	*73%*
$P_{ABSORBED}$	1.25kW	*100%*	$P_{ABSORBED}$	2.5kW	*200%*
Cable Losses	14.4kW	*100%*	Cable Losses	7.2kW	*50%*

Price: → ↑ ↗

4 Quadrant Operation: Receptor mode

Goals:

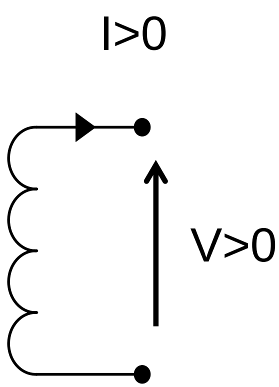
- Absorbing magnet energy
- Still regulating magnet reverse voltage, i.e dI/dt



•Solutions:

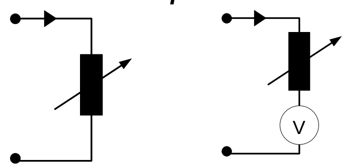
Ideal Magnet

No Resistance

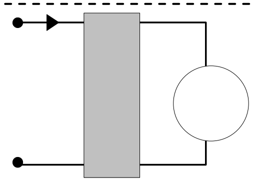


Energy Receptor

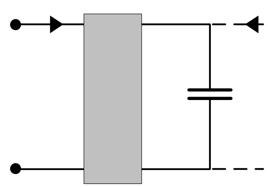
Concepts



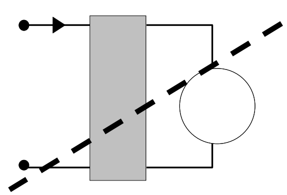
- Variable resistor (active)
- Voltage source added for 0 A transition: No voltage can be obtained when 0 Amp in the magnet.



- Converter magnet-mains, giving back energy to mains.



- Converter magnet-capacitor, storing the magnet energy.
- This capacitor is charged by the magnet and the needed generator converter



•*Alternative (not very used) solutions could be: rotative machine, or (supraconductor) inductor…not treated here.*

4 Q Stage: Main topologies

2x Thyristor bridge in anti//

Very well known

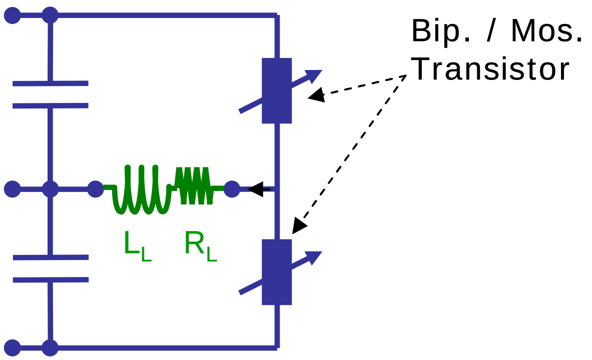
Power returned to mains

Linear dissipative Stage

Basic background known, (push-pull stage)

4Q operation to be explained later

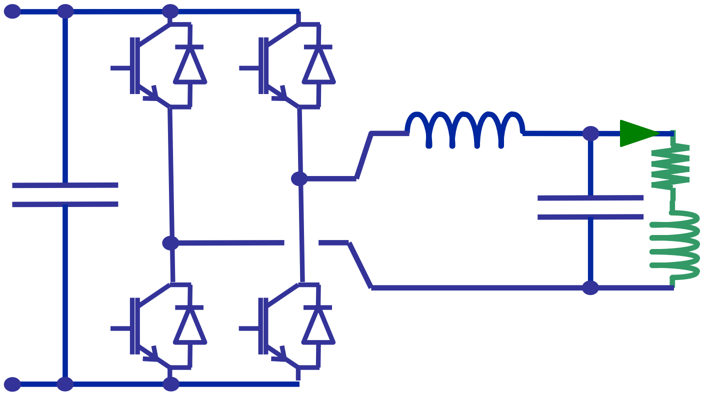
Dissipation in the transistors, acting as programmable resistor



Switching Stage

Conventional H bridge (L-C Filter)

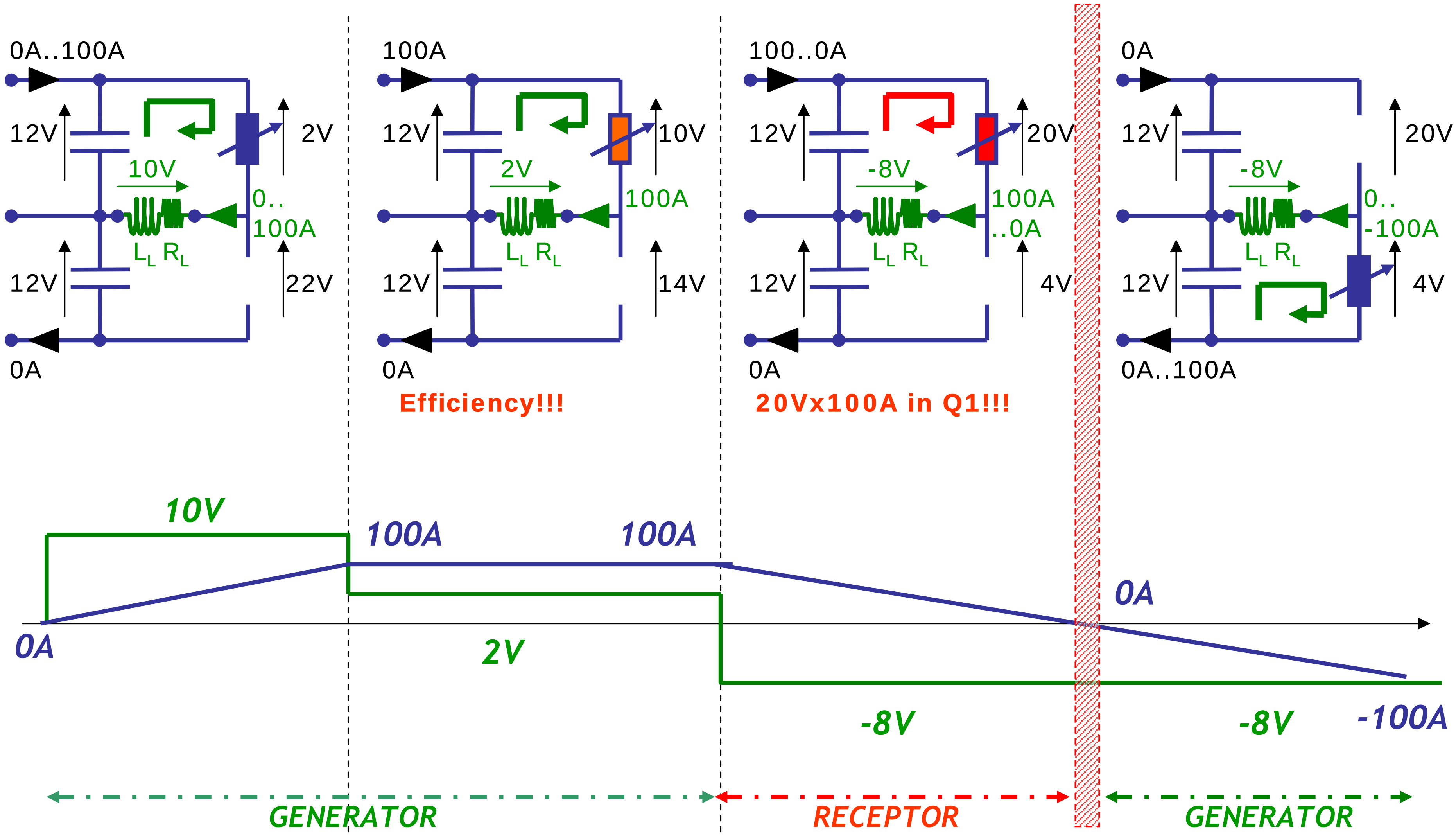
Power returned to capacitor or dissipated in brake chopper.



4Q Stage: Linear basic principle

(* The 2 voltages are always the same)

…Combined with double* DC fixed voltage output

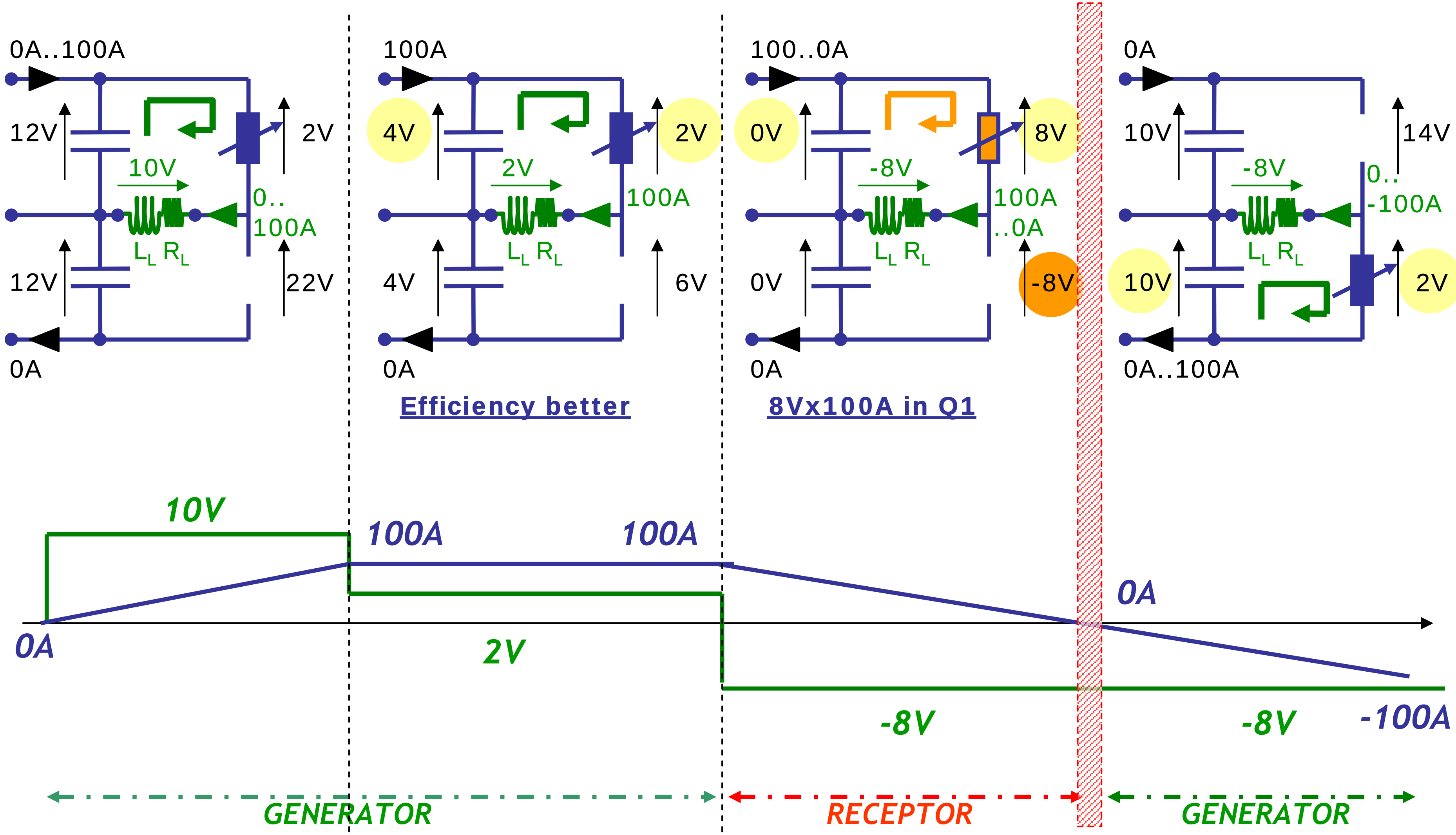


4Q Stage: Linear basic principle

(* The 2 voltages are always the same)

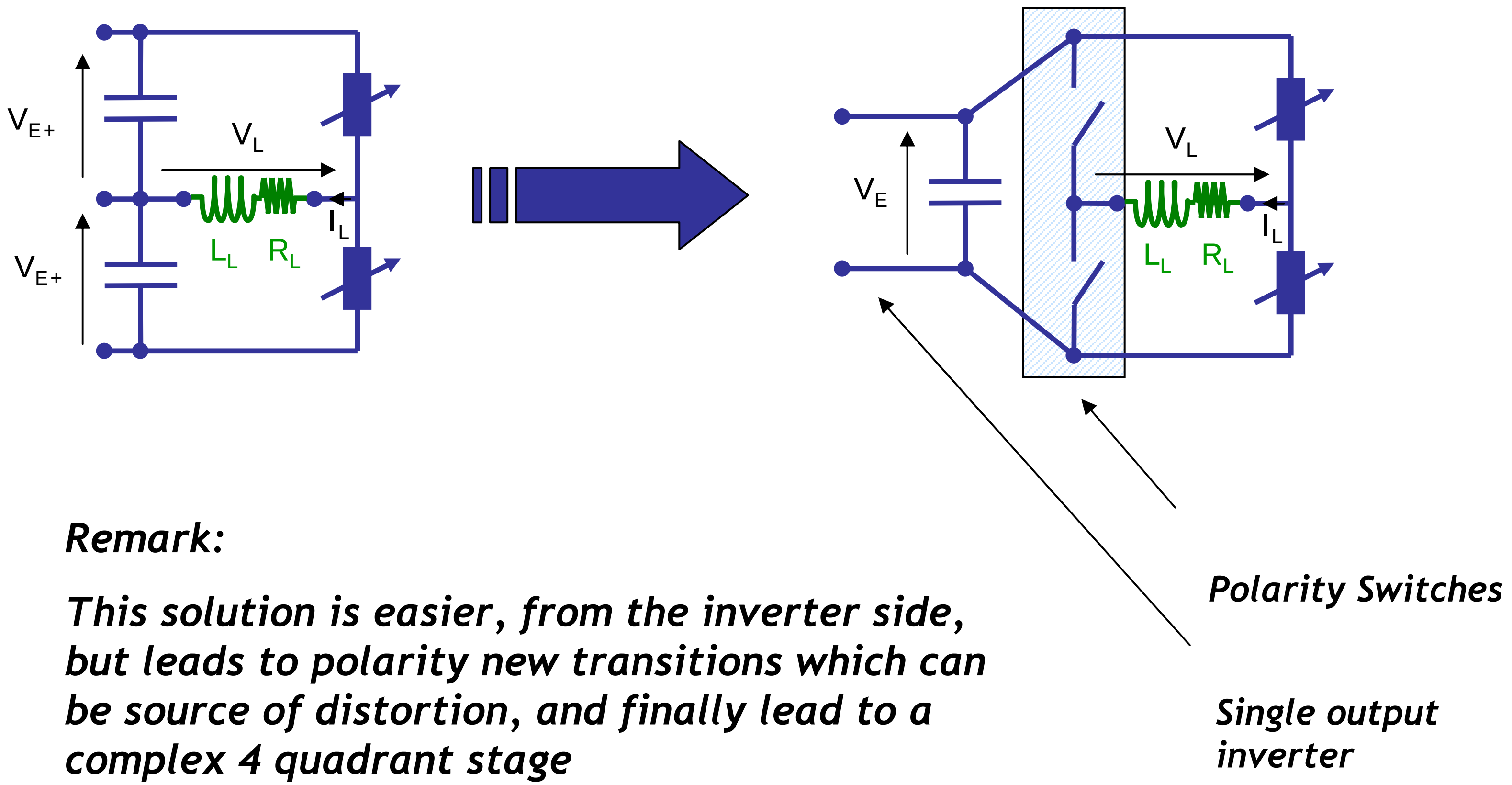
…combined with double* DC variable voltage output

for better efficiency an losses reduced in receptor mode



4Q Stage: Linear basic principle (variation "linear" H bridge)

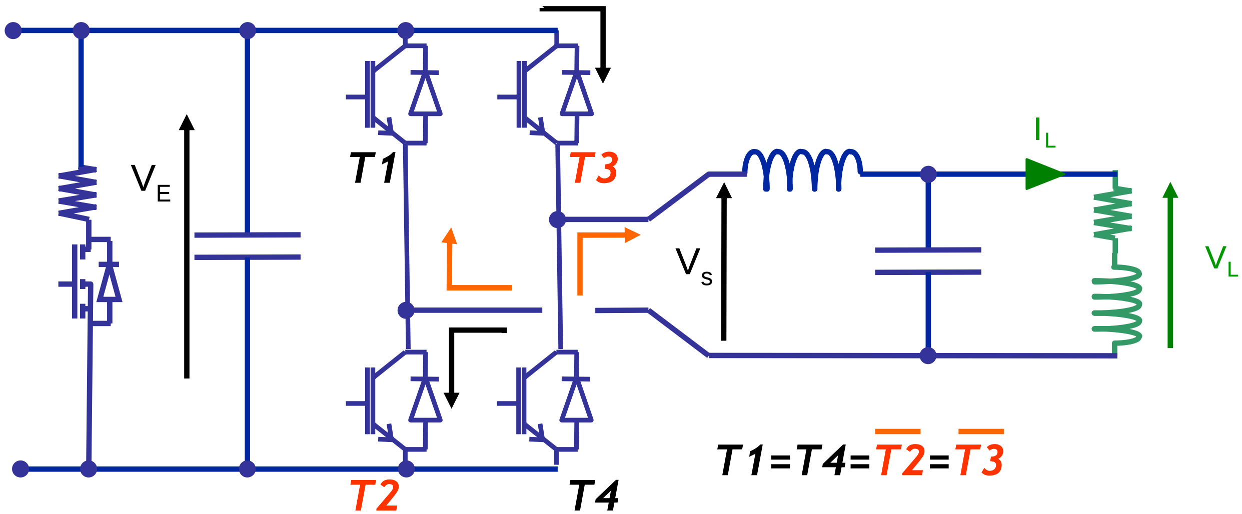
…combined with single DC variable voltage output

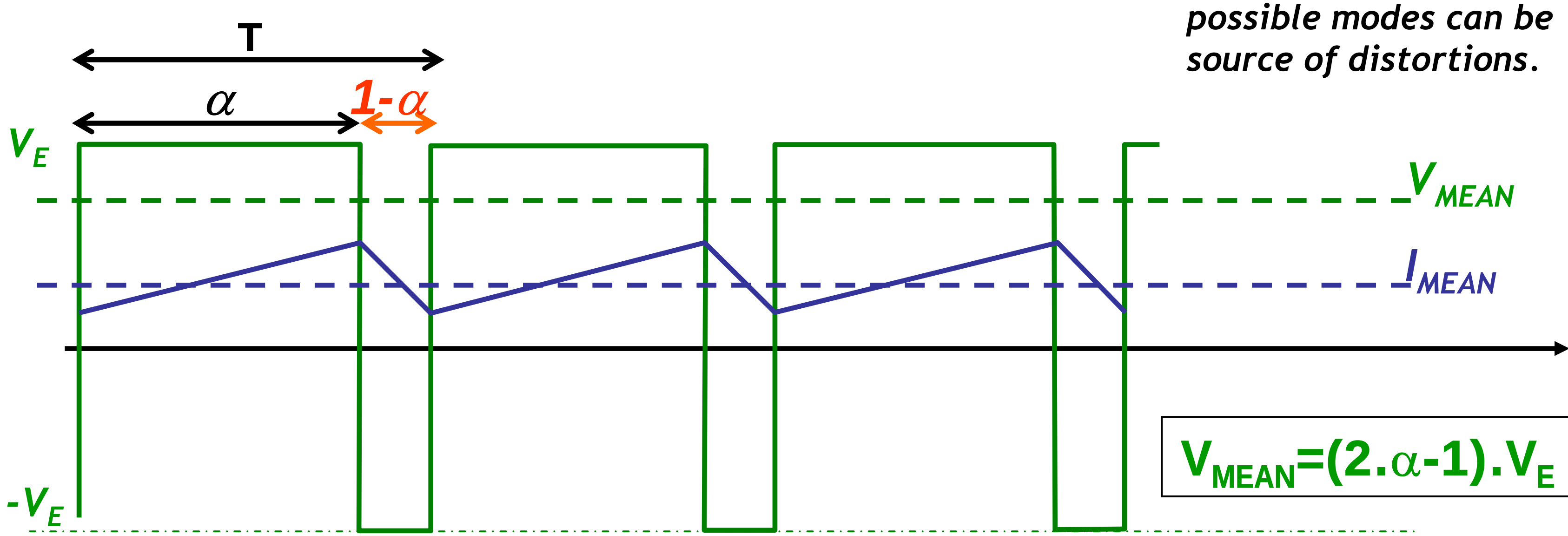


Remark:

This solution is easier, from the inverter side, but leads to polarity new transitions which can be source of distortion, and finally lead to a complex 4 quadrant stage

4Q Stage: Switching basic principle





$$\boxed{V_{MEAN}=(2.\alpha-1).V_E}$$

H Bridge: 2 modes

It is possible to work in Buck Mode so that both

- Δ I is reduced (HF output voltage ripple)

- Losses are reduced

Note:
transition between these 2 possible modes can be source of distortions.

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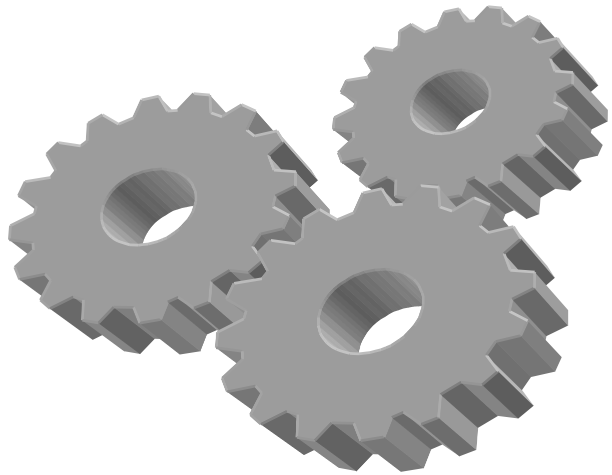
Topologies: Key points, (how to classify them, how to select them?)

SIZE, WEIGHT,
COST

POWER RANGE,
DISSIPATIVE OR NOT,
EFFICIENCY

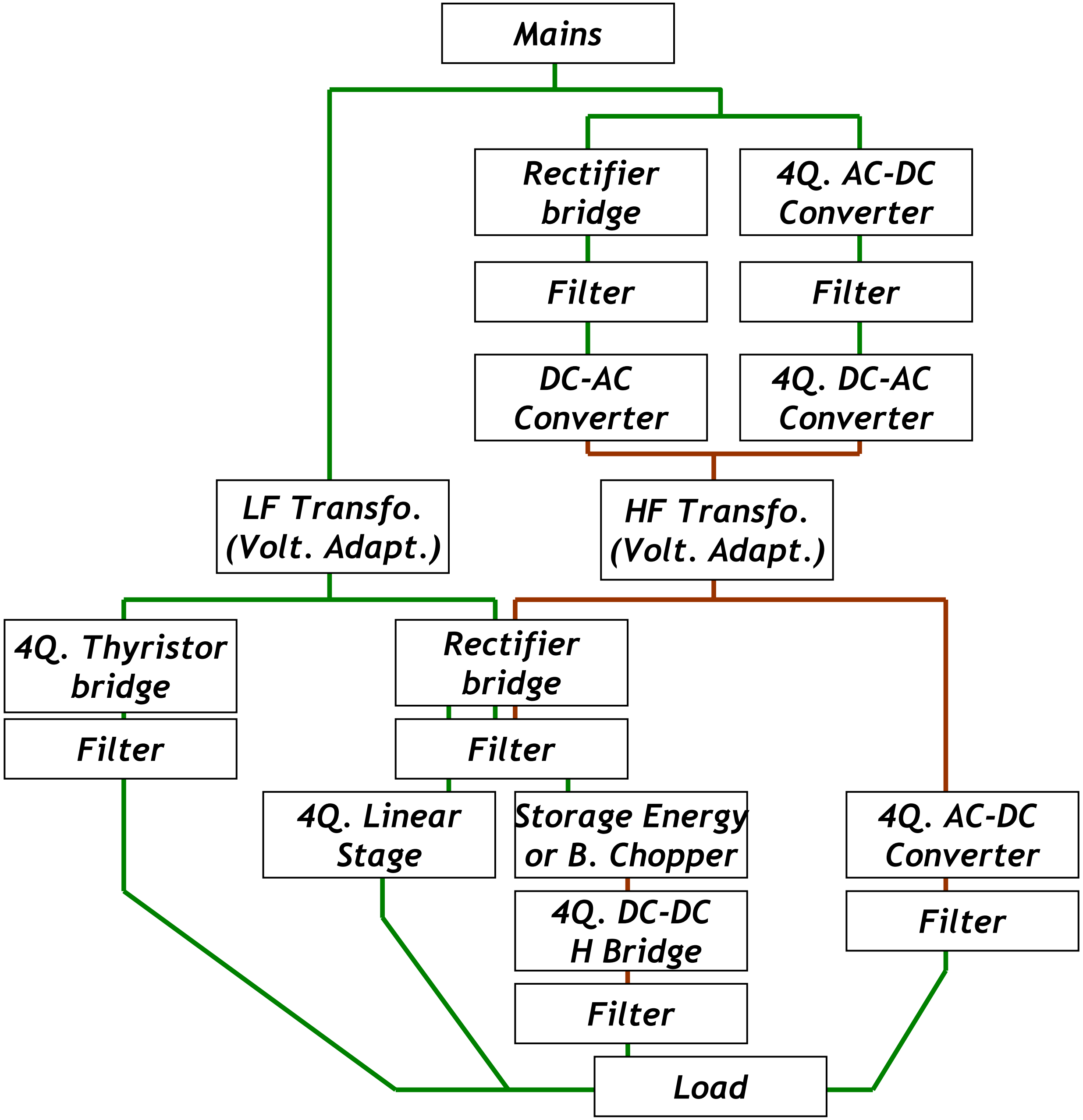


AC MAINS PERT. REJ.,
EMC, BF & HF RIPPLE

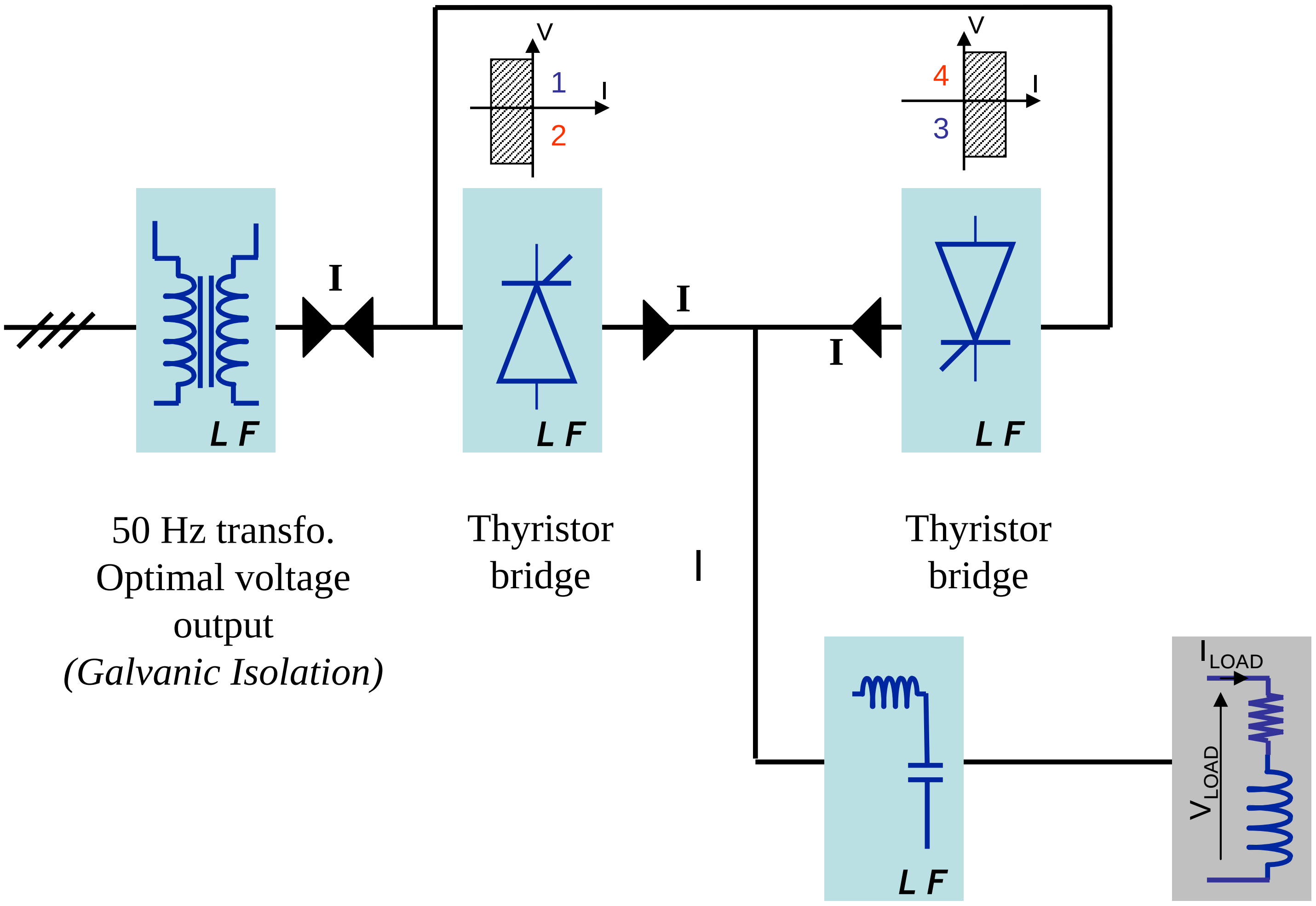
TOPOLOGY CHOICE ????

NUMBER OF CPTS, DESIGN
COMPLEXITY, MTBF, USE OF
COMMERCIAL PART

DISTORTION
BANDWIDTH


Mains
Rectifier bridge
4Q. AC-DC Converter
Filter
Filter
DC-AC Converter
4Q. DC-AC Converter
LF Transfo. (Volt. Adapt.)
HF Transfo. (Volt. Adapt.)
4Q. Thyristor bridge
Rectifier bridge
Filter
Filter
4Q. Linear Stage
Storage Energy or B. Chopper
4Q. AC-DC Converter
4Q. DC-DC H Bridge
Filter
Filter
Load

Topologies: Thyristor (Principle)



50 Hz transfo.
Optimal voltage
output
(Galvanic Isolation)

Thyristor
bridge

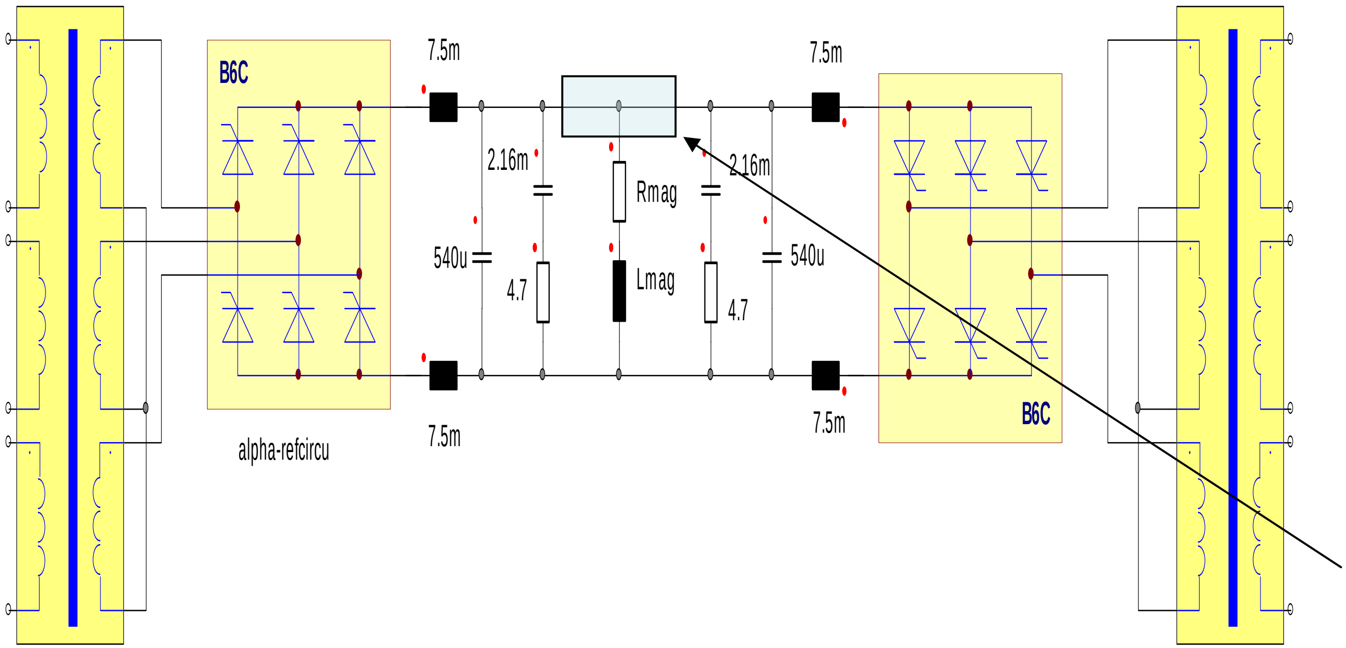
Thyristor
bridge

Low freq.
Output Filter

Topologies: Thyristor (schematics Example)

Basic schematic

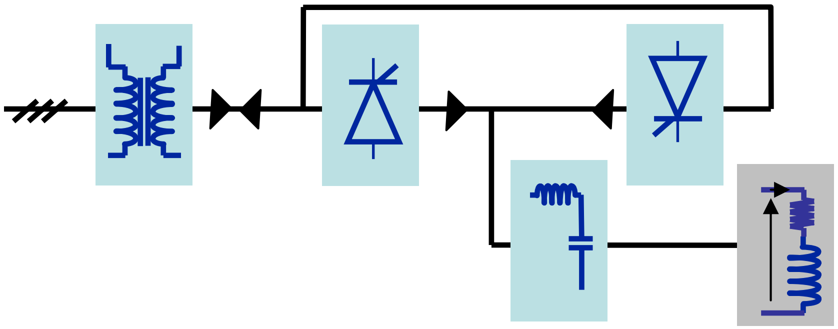
• [0,0] & [V] axis required circulating current between the 2 bridges



• Active Filter increase dynamic performance (low amplitude bandwidth, low frequency ripple, perturbation…)

Adding a circulating current between the 2 thyristor bridges helps!!!

Topologies: Thyristor (Discussion)



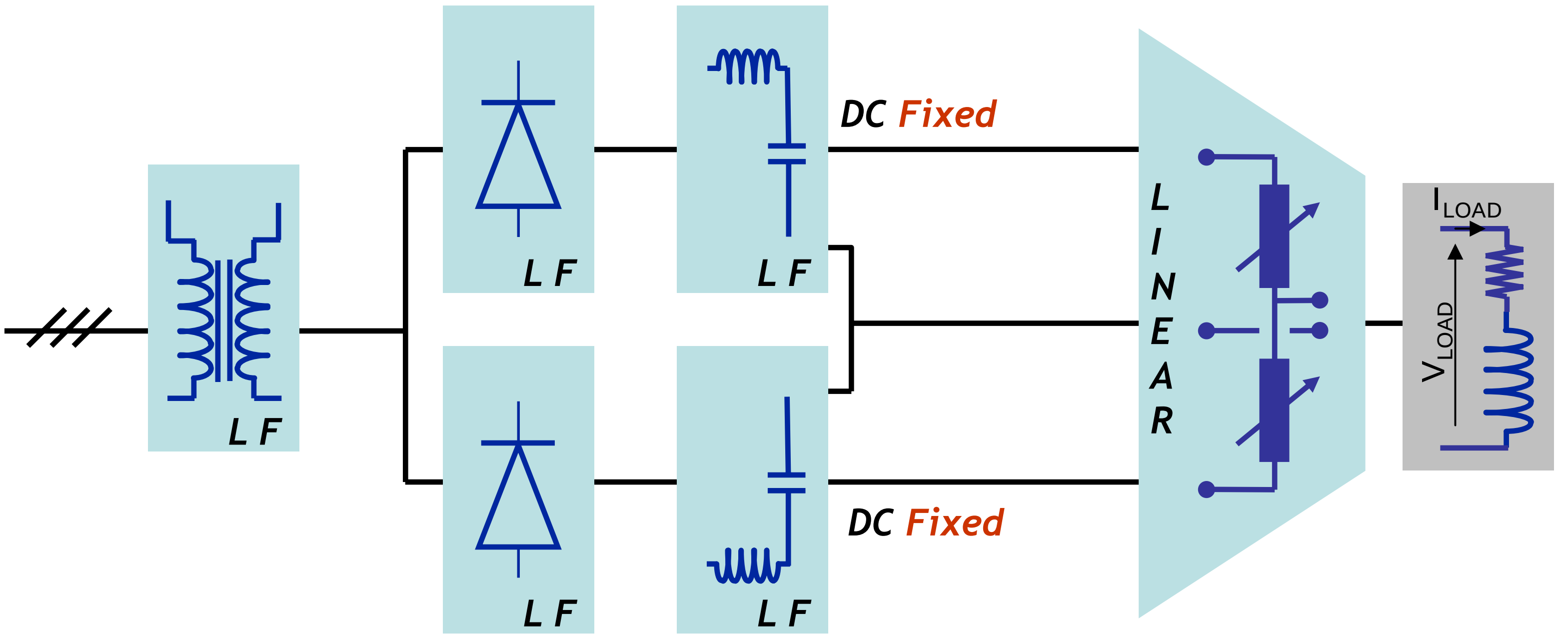
Advantages

- Huge power possible
- Not Dissipative: power returned to mains
- High Efficiency
- Very well known topology
- Rather simple design
- No High frequency signal (low frequency operation): EMC easy to handle

Drawbacks

- Low Bandwidth (addition of active filter can help a bit in small signal)
- Poor AC mains perturbation rejection (speed loop limited by L-C filter)
- Distortion (crossing axes, and point [0,0]) requires some additional circuit for high precision converter: Circulating current
- Size, weight of transformer and filtering elements

Topologies: 50Hz + Linear (Principle)

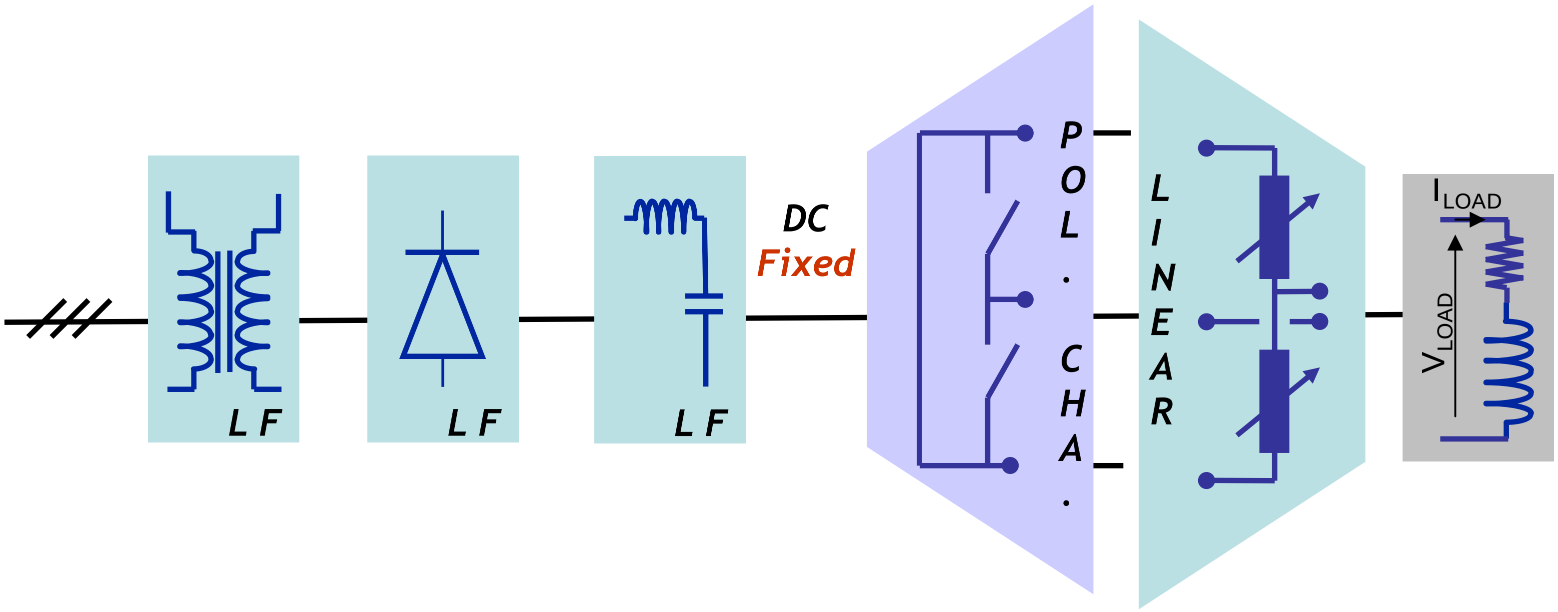


50 Hz transfo.
Optimal voltage
output
(Galvanic Isolation)

Rectifier +
Double Output
High Freq.
Filter

Linear Stage
(Dissipate Magnet Energy)

Topologies: 50Hz + Linear (Principle *variation*)



50 Hz transfo.
Optimal voltage
output
(Galvanic Isolation)

Diode
bridge

Low freq.
Output Filter

H Bridge
Linear Stage
(Polarity Changer
/
Dissipate Magnet
Energy)

Topologies: 50Hz + Linear (Discussion)

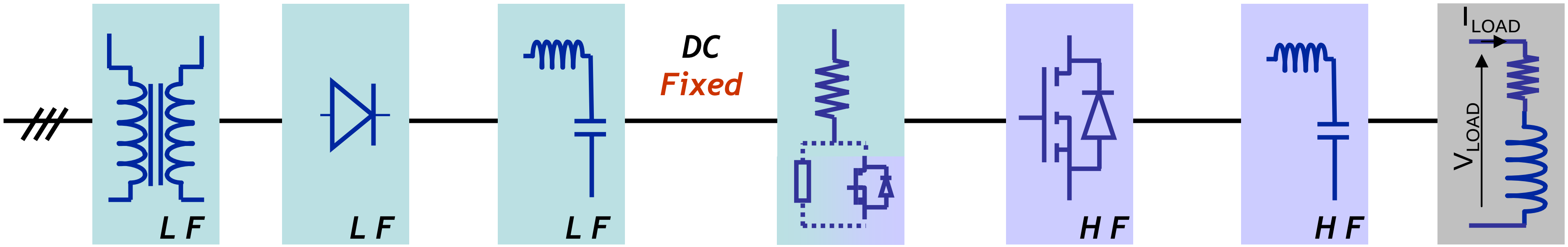
Advantages

- Schematics and topologies are very well known
- Simple schematics
- Adding circulation current helps
- Bandwidth (10 kHz)

Drawbacks

- Dissipative
- Efficiency very low in generator mode
- Size, weight of transformer and filtering elements
- Often realized with several transistors in // (MTBF and avalanche failure)

Topologies: 50Hz + Switching (Principle)



50 Hz transfo.
Optimal voltage
output
(Galvanic Isolation)

Diode
bridge

Low freq.
Output Filter
(Magnet Energy
➔1/2.C.V²)

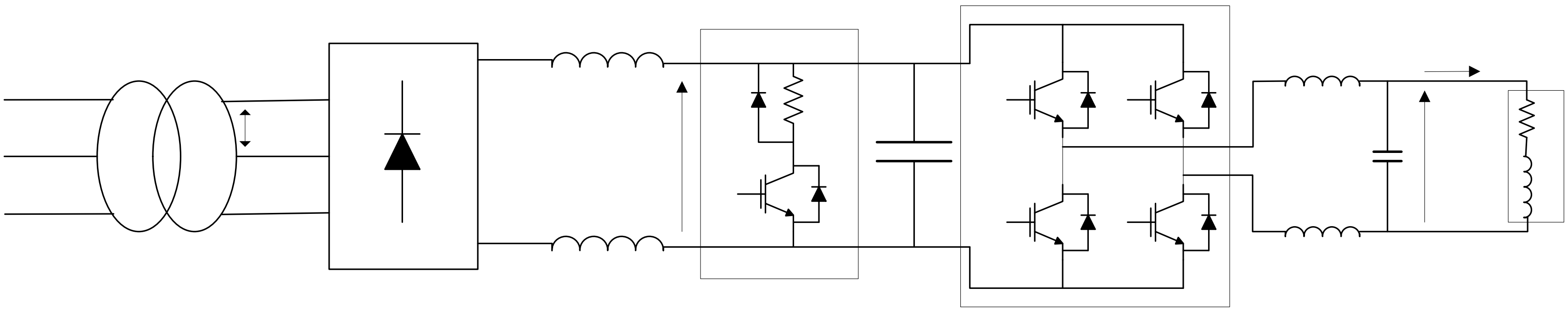
Add.
Brake Chopper
(Optional)
(Dissipate Magnet
Energy)

PWM
Converter
Hard
Commutation

High freq.
Output Filter

Topologies: 50Hz + Switching (Schematics Example)

Basic schematic



50Hz Transfo + L -C Filter

Rectifier bridge

High Frequency Hard commutation Bridge

+

$L_F/2$

Commercial part possible

R

V_{DCin}

400V ~ 50 Hz

S

T

Δ Y

UII

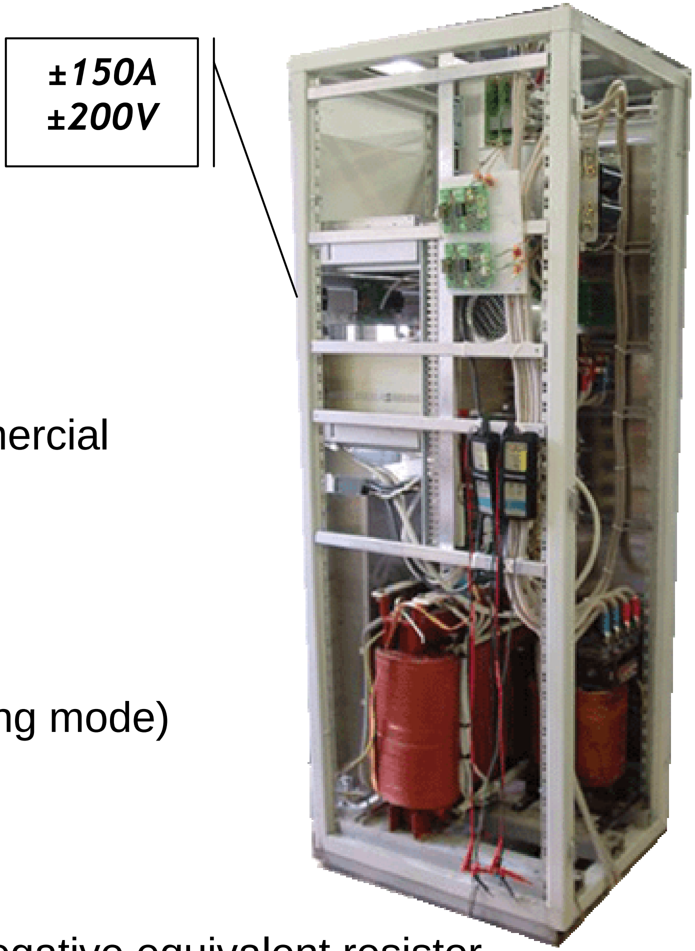
Brake chopper: absorb magnet energy if Vcap. too high

High Frequency LC Filter (2 cells)

-

$L_F/2$

Topologies: 50Hz + Switching (Discussion)



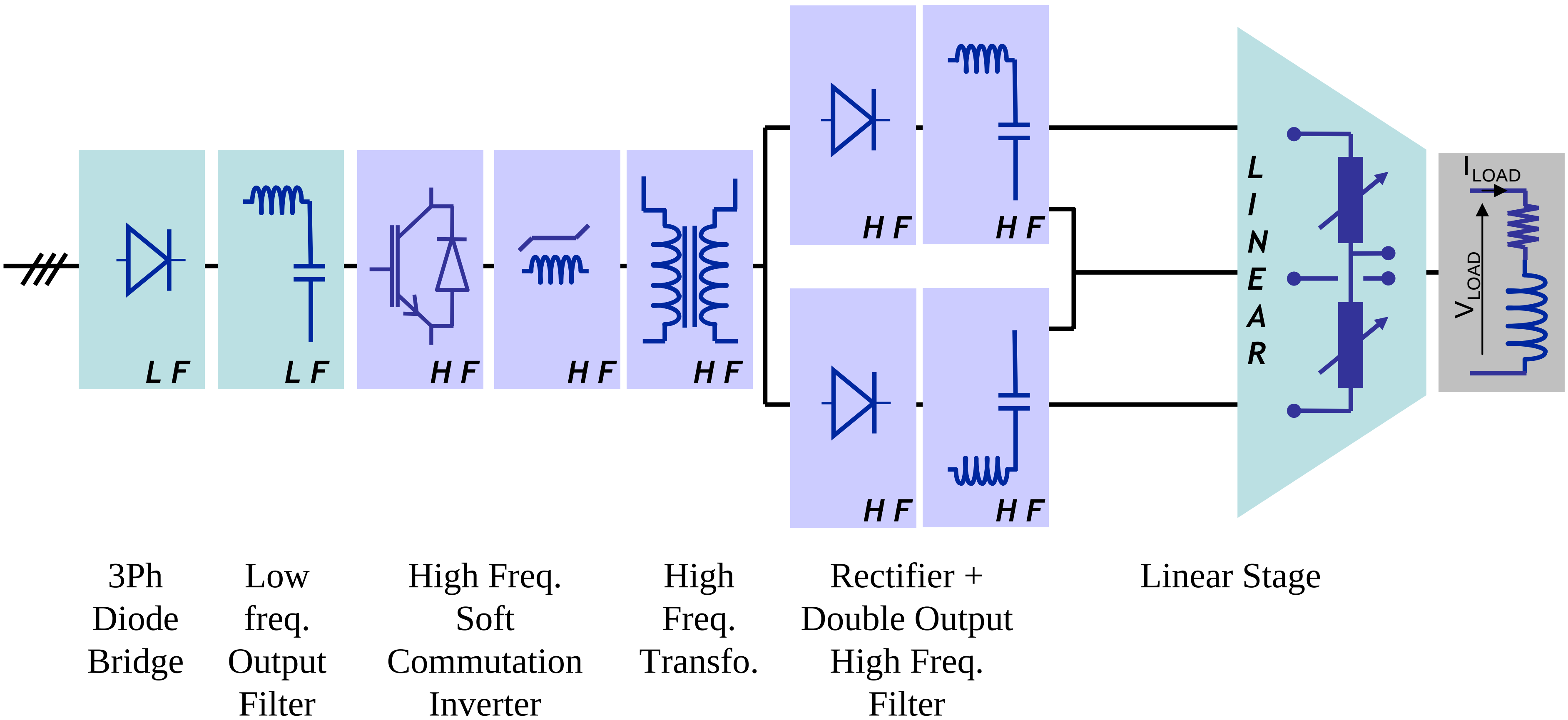
Advantages

- Huge power possible
- Part of magnet energy re-used
- Very well known topology– possible to use commercial standard elements
- High bandwidth (10 kHz)
- Good AC mains perturbation rejection
- No distortion of the signal (if H bridge not changing mode)

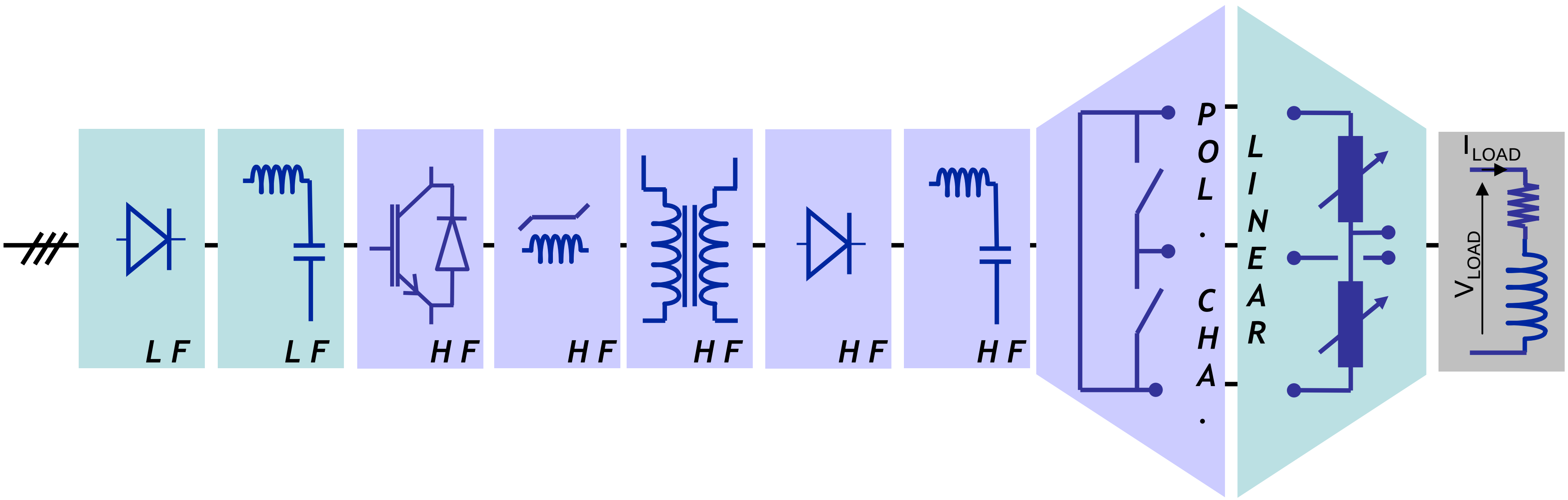
Drawbacks

- H bridge hard commutation @ high current
- 50Hz LC-Filter can be un-damped by H bridge negative equivalent resistor
- Size, weight of transformer and filtering elements
- Hard commutation EMC to cope with
- Low voltage high current not ideal (loss of the switching H bridge, $f_{switching}$ limited)
- HF filtering Ripple difficult (if buck mode not used), at “only $f_{switching}$”

Topologies: Switching + Linear (Principle)



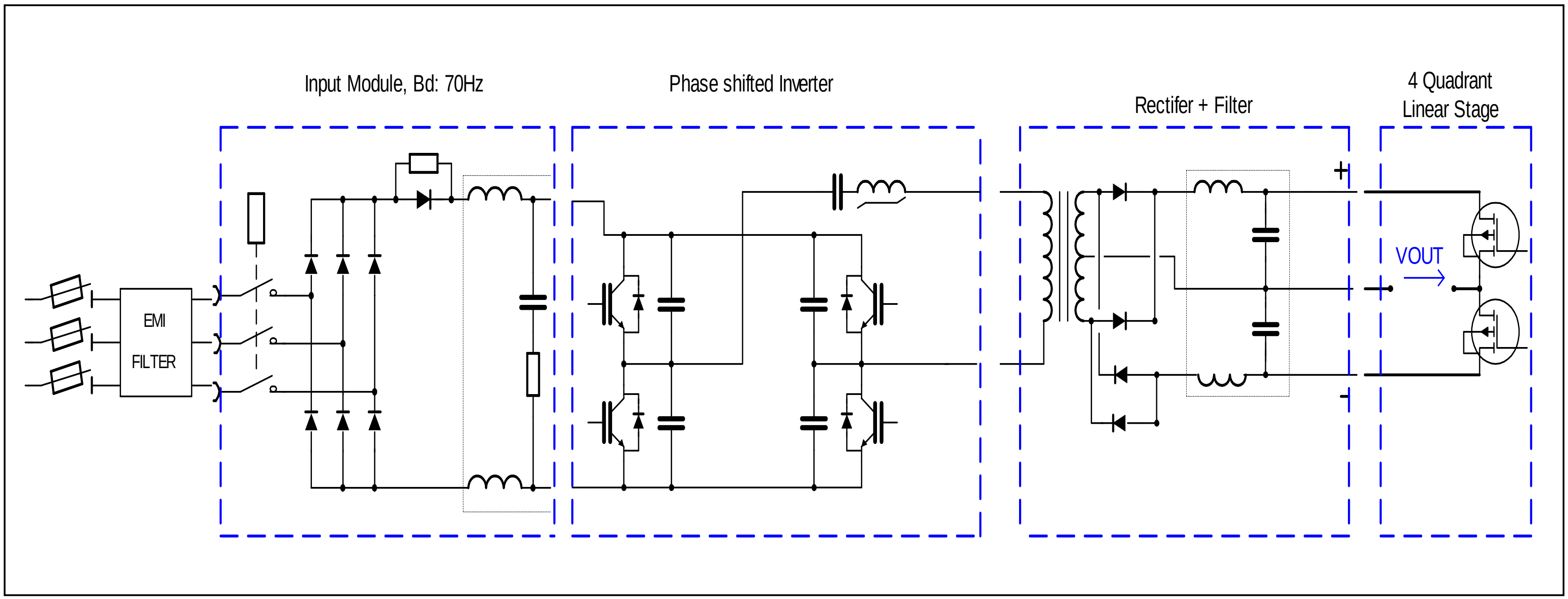
Topologies: Switching + Linear (Principle *variation*)



3Ph Diode Bridge	Low freq. Output Filter	High Freq. Soft Commutation Inverter	High Freq. Transfo.	Rectifier + Single Output High Freq. Filter	H Bridge Linear Stage *(Polarity Changer)*

Topologies: Switching + Linear (Schematics Example)

Basic schematic



300Hz L -C Filter

High Frequency Soft commutation H Bridge

HF Transfo.

HF Filter + Rectifier

4Q Linear Stage

Topologies: Switching + Linear (Discussion)

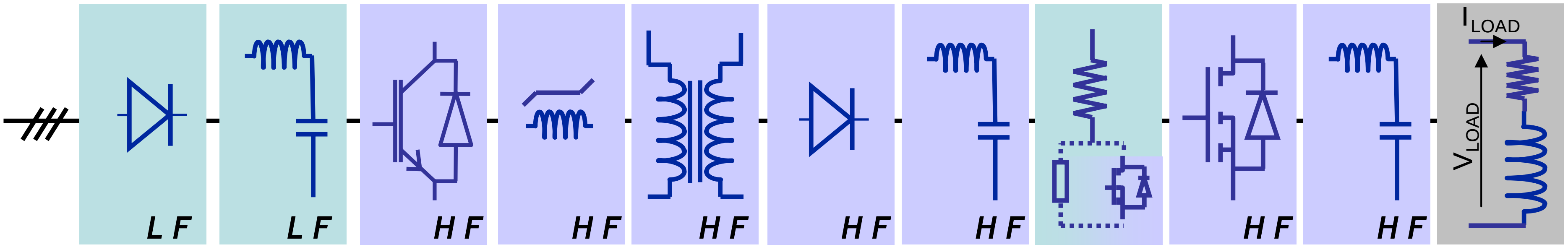
Advantages

- Medium power possible
- Addition of 2 distinct well known topologies
- High bandwidth
- Good AC mains perturbation rejection
- No distortion of the signal (if circulating current used)
- HF filtering Ripple at 2x $f_{switching}$ possible
- Efficiency OK, (no switching Loss at secondary side)
- EMC OK, since Soft commutation possible

Drawbacks

- Dealing with Inverter Loop & Circulation current Loop can lead to some complexity
- Double output voltage requires additional power components (L-C Filtering + Rectifiers)
- Dissipative (No energy back to anywhere, except Output transistors!!!)

Topologies: Switching + Switching Type 1 (Principle)



50 Hz transformer
Optimal voltage output
Galvanic isolation

Diode
bridge

Low freq.
Output Filter

Add.
Crowbar

PWM Converter
Hard Commutation

Topologies: Switching + Switching Type 1 (Discussion)

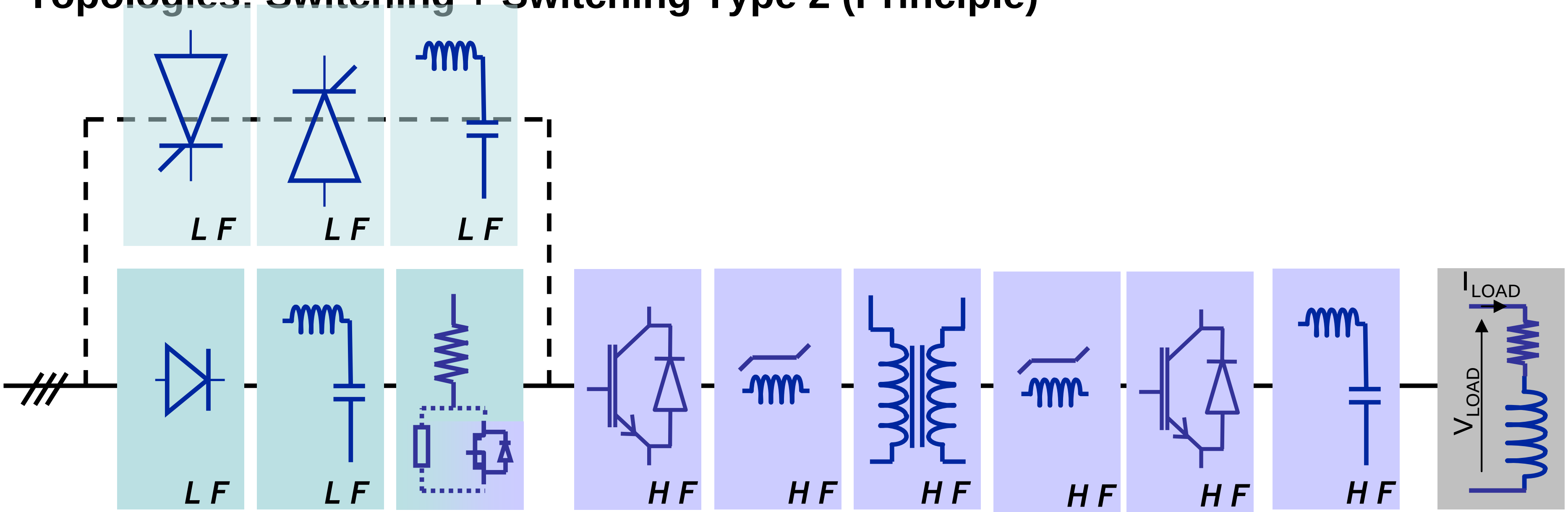
Advantages

- High power possible
- Part of magnet energy re-used
- Very well known topology
- High bandwidth
- Good AC mains perturbation rejection
- No distortion of the signal (if H bridge not changing mode)

Drawbacks

- Secondary H bridge hard commutation @ high current (Losses EMC to cope with)
- Low voltage high current not ideal (loss of the switching H bridge, $f_{switching}$ limited)
- 2 HF filtering levels
- Complexity (2 inverters, Gate drives) & Cost
- Efficiency low
- HF filtering Ripple difficult (if buck mode not used), at “only $f_{switching}$”

Topologies: Switching + Switching Type 2 (Principle)



Diode bridge

Low freq. Output Filter

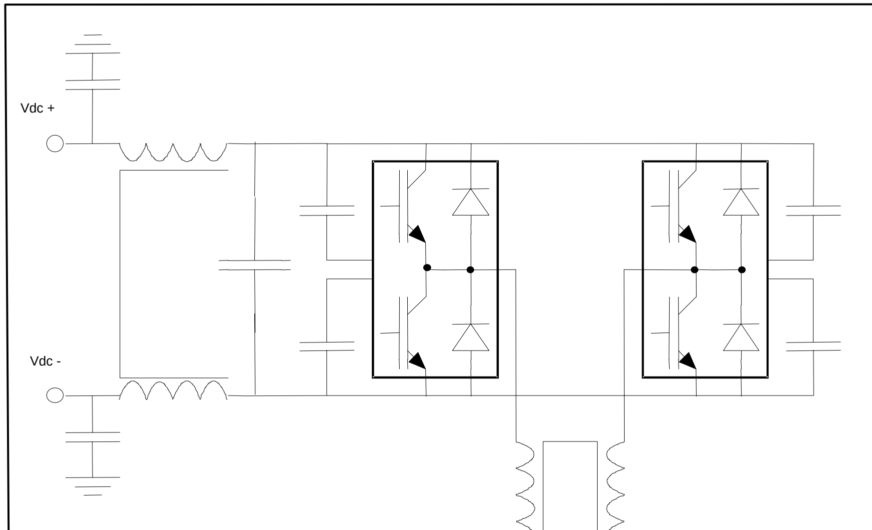
Add. Crowbar

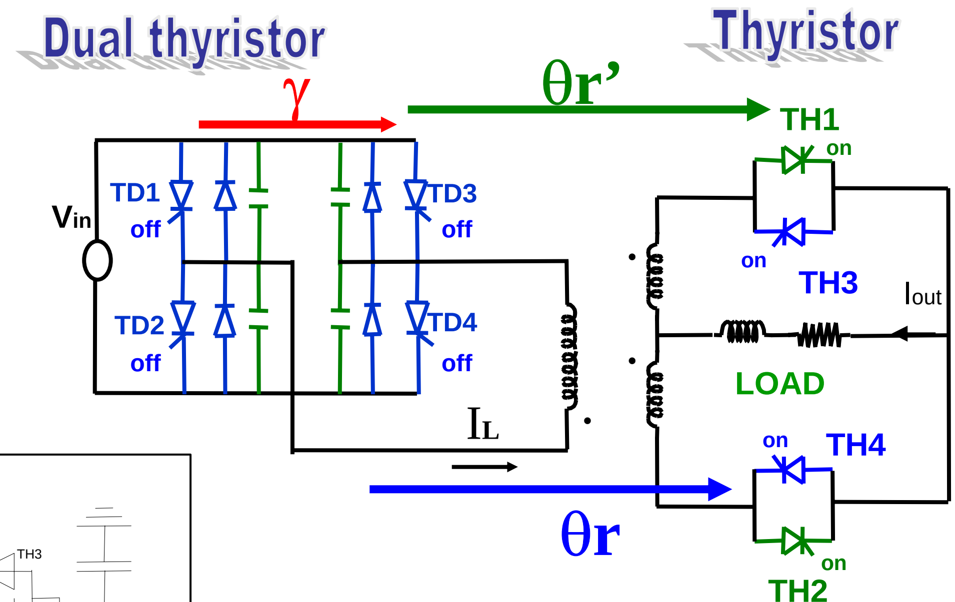
High Freq. Soft Commutation Inverter

High Freq. Transfo.

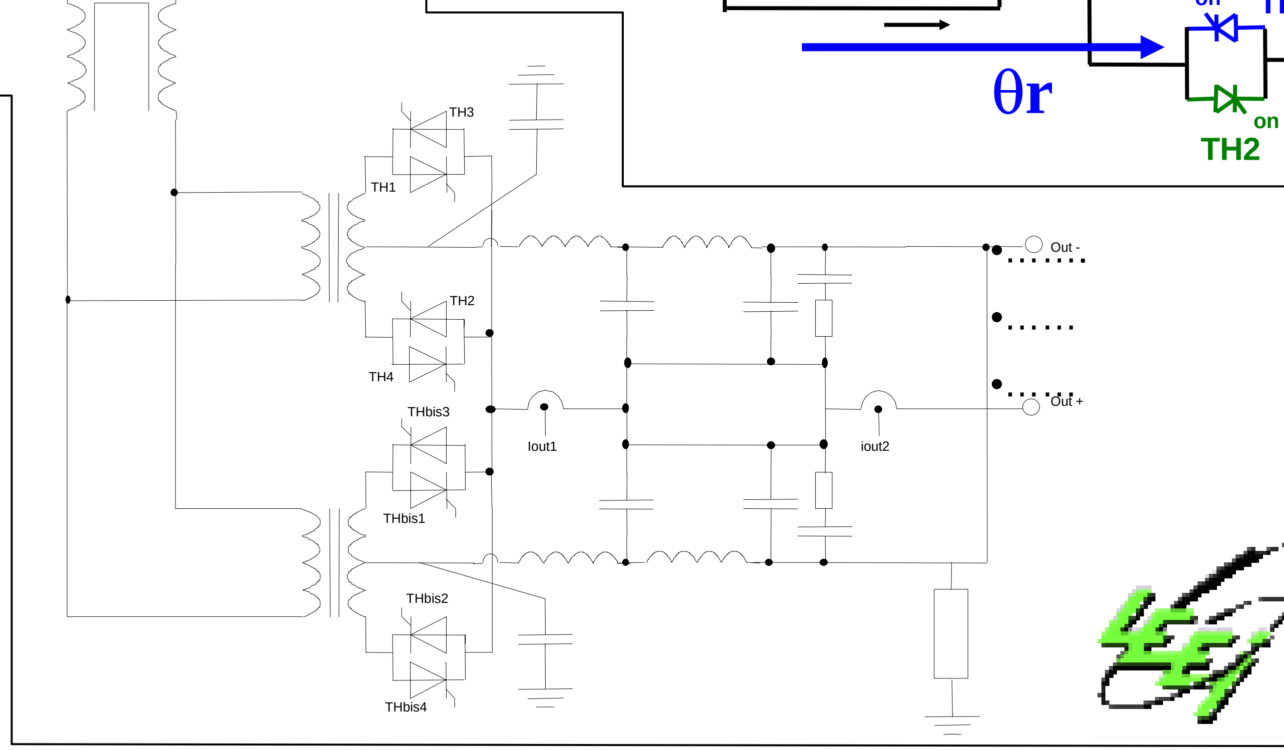
4Q Converter Soft Commutation

Topologies: Switching + Switching Type 2 (Schematic Example)





See Paper from CERN & LEEI for detailed explanation.



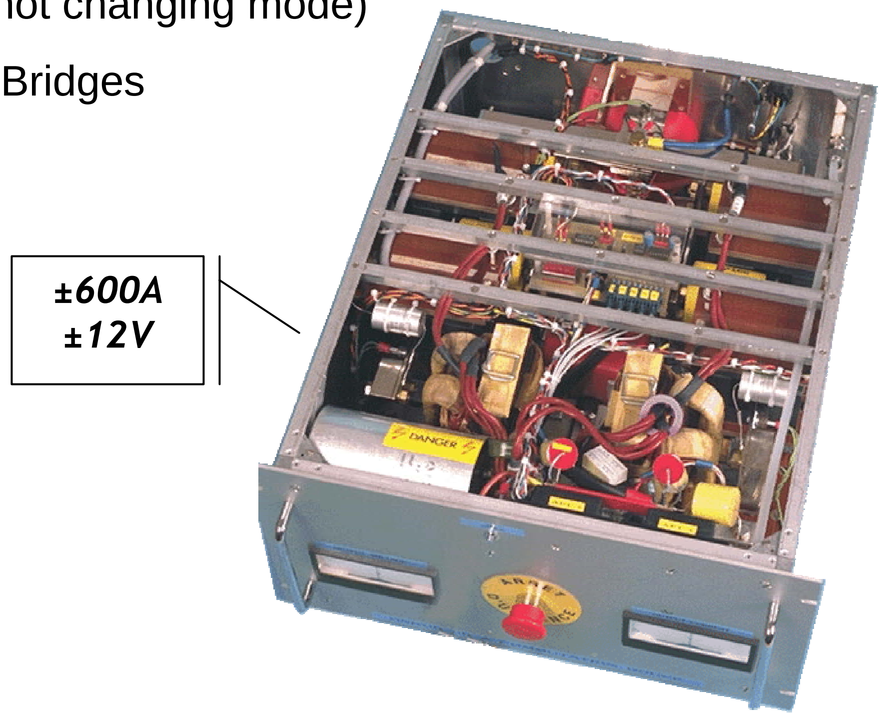
Topologies: Switching + Switching Type 2 (Discussion)

Advantages

- Fully reversible with energy sent back to mains (thyristor bridge to be added)
- High frequency power converter (low volume and high dynamic performance)
- High bandwidth
- Good AC mains perturbation rejection
- No distortion of the signal (if H bridge not changing mode)
- Soft commutation possible on the 2 H-Bridges
- High efficiency

Drawbacks

- Complex control



4 Quadrant basic background

- 4Q. Conventions
- 4Q. Working area / loads
- 4Q. Basic schematics

4 Quadrant topologies Review

- Principle schematics (main ones presented)
- Advantages / Drawbacks
- Some realizations

4 Quadrant practical realization & example

- LHC Specifications
- LHC Topology choice explained
- LHC Converter principles
- Technical points highlighted (loops, circulating current,…)
- Realizations

LHC: Specifications

- Electrical Characteristics
  - Low Output Voltage / High Output Current
  - High Efficiency (Losses in Tunnel must be as low as possible)
  - High bandwidth
  - No need for returning power to mains (slow machine)
  - Operation close to [0V-0A]
  - Low BF ripple (magnet current precision) & Low HF Ripple (EMC)
- Mechanical Characteristics
  - To be installed in LHC tunnel
  - Must be possible to change it as a plug-in module
  - Low volume and low weight
- Electrical Environment
  - Good immunity to mains perturbation (phase loss of 100ms)
  - Very low level of distortion tolerated (high precision)
  - EMC behavior must be very good (IN & OUT)
  - To be integrated in a few ppm current loop regulation
- Other key points
  - 15 years of operation (MTBF)
  - Principle as simple as possible (operation)

LHC Power Converters Family

LHC ±600A ±40V
Transtechnik
Germany
50 Units

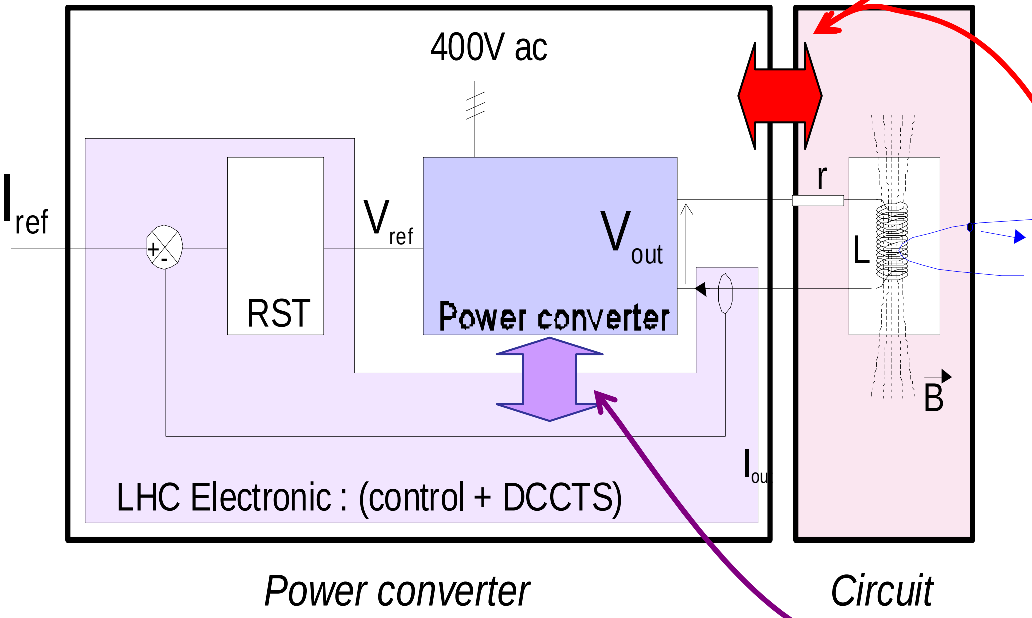
LHC ±600A ±10V
Cirtem
France
440 Units

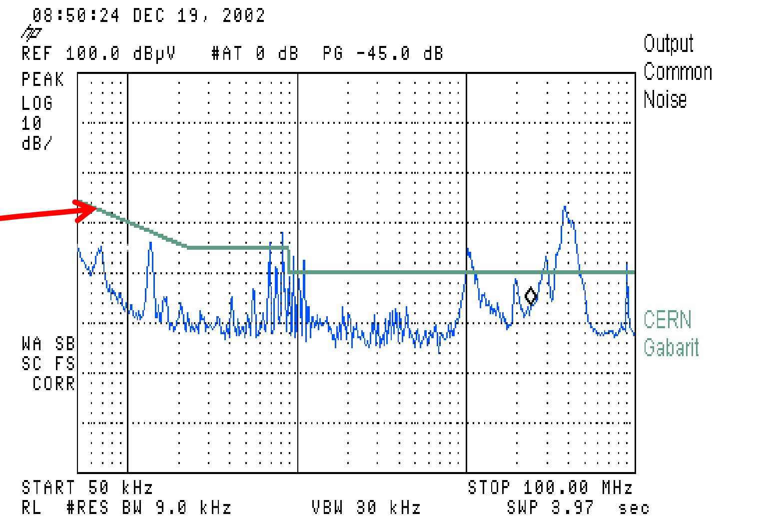
LHC ±120A ±10V
CERN & EFACEC
Portugal
330 Units

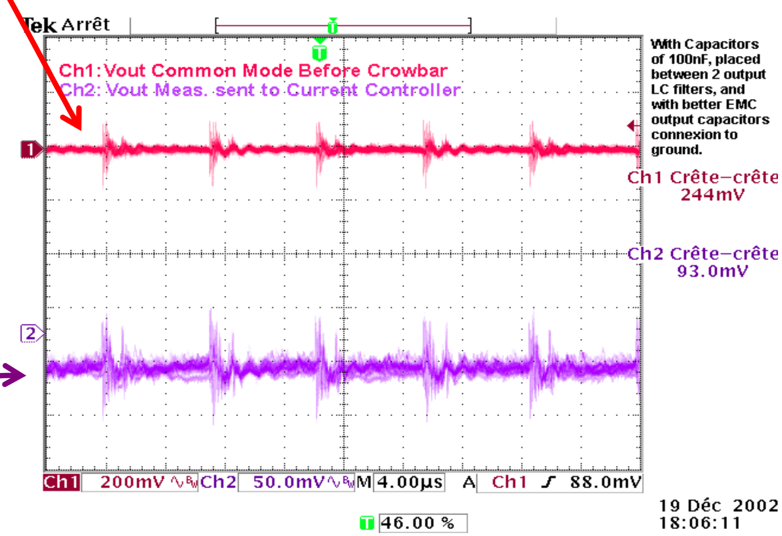
LHC ±60A ±08V
CERN & CEL
France
800 Units

LHC ±120A ±10V: EMC *Highlighted*

Magnet loads are several magnets in series
(hundreds of meters "load")
IEC478.3 C applied INPUT and OUTPUT side







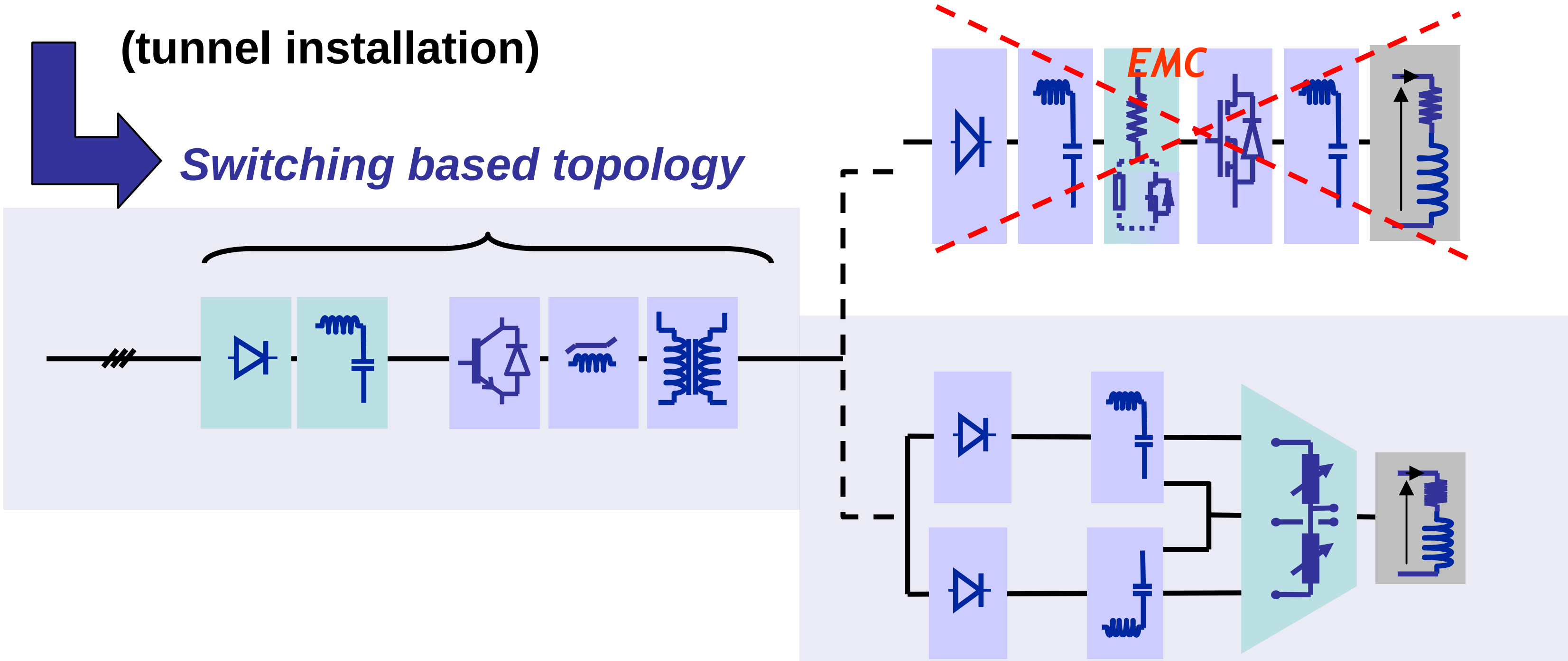
Digital & Analog signals exchanged between
Power converter
& High Precision Current Controller

LHC ±120A ±10V Topology Choice

Minimum 50Hz Components for size & weight reduction

(tunnel installation)

Switching based topology



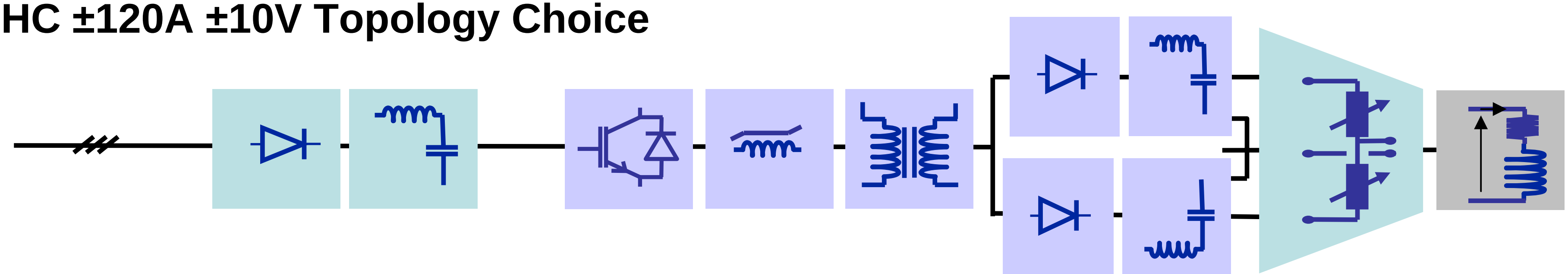
Linear base topology

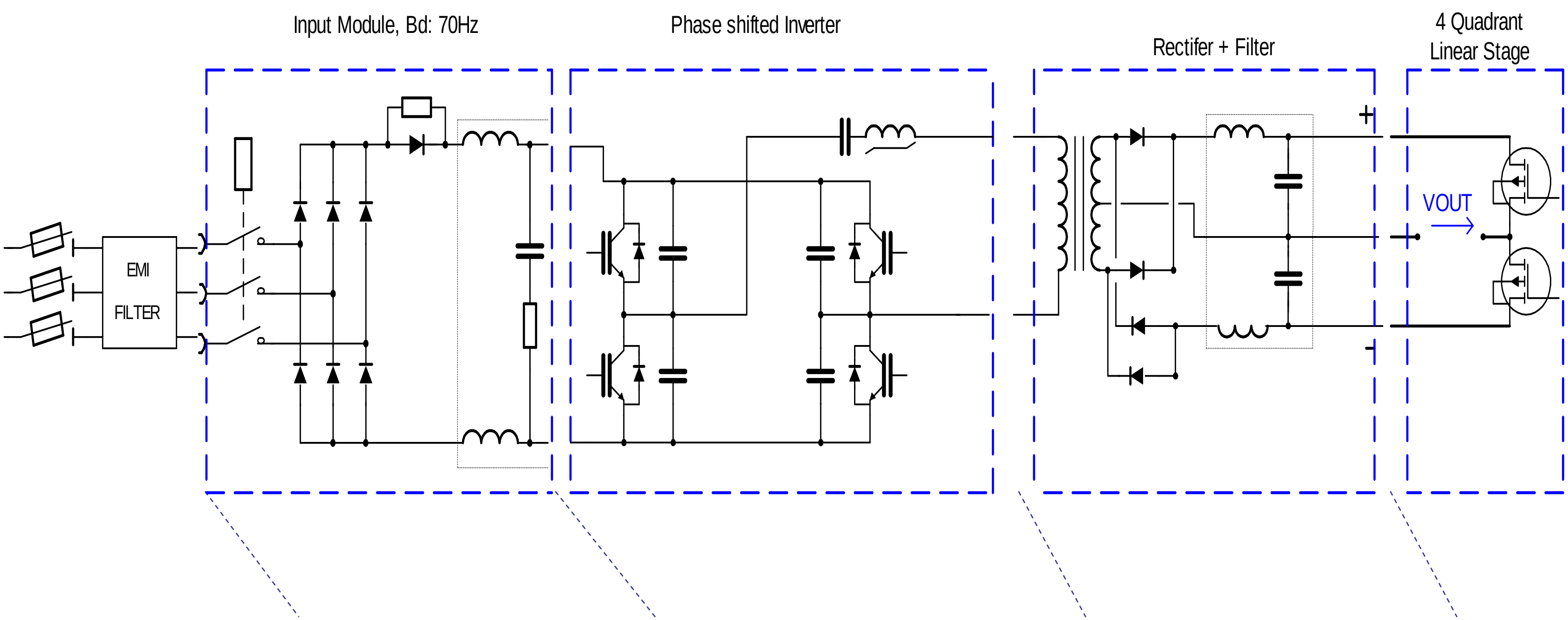
High precision environment:

EMC must be as good as possible

No distortion / operation [0V-0A]

LHC ±120A ±10V Topology Choice



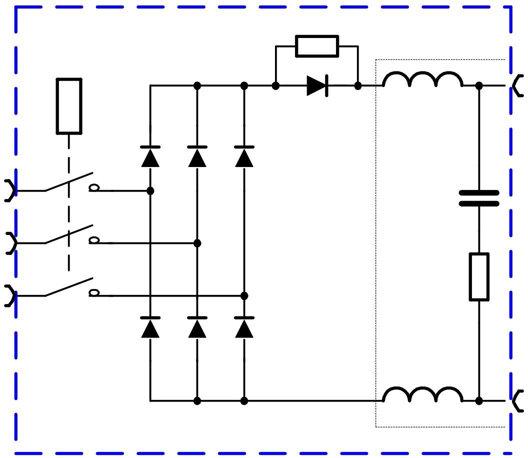


BREAKER & CONTACTOR	INPUT FILTER & SOFT-START	SOFT COM. INVERTER, 50kHz..100kHz	ISOLATION & RECTIFIER + FILTER	4Q.L.S.

LHC ±120A ±10V Topology Choice

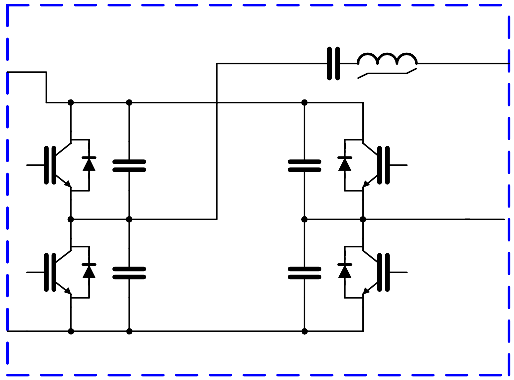
AC-DC

- 3 phases + Neutral (used for auxiliary power supply)
- 1400V Rectifiers
- 70Hz Input filter (damped with C-4C) to give a flat 540V DC (around -20dB on 300Hz)
- Soft start based on “R + switch”.



High Frequency Soft commutation Inverter

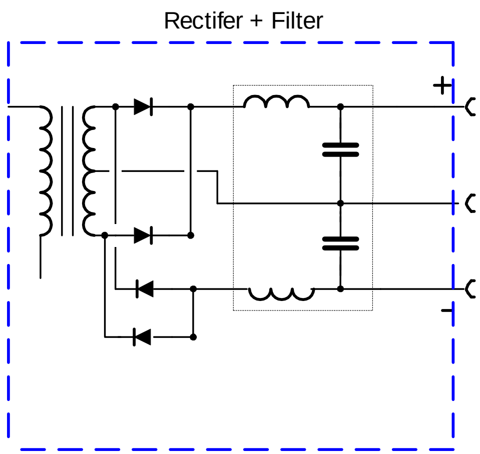
- Fixed switching frequency (50..100kHz).
- ZVS operation with Phase Shifted command.
- ZCS for lagging leg
- IGBT Bridge
- “Voltage” or “current” mode possible



LHC ±120A ±10V Topology Choice

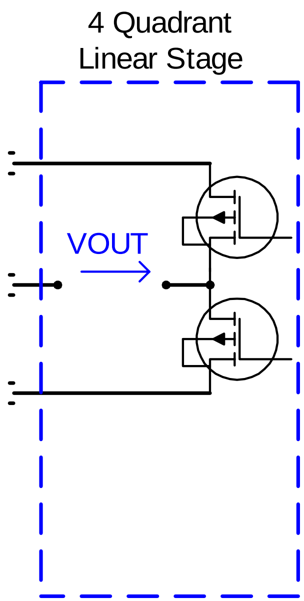
Rectifier + DC Filter

- HF Ripple at 2x inverter $F_{switching}$
- Schottky rectifiers.
- Double LC cell at 5..10 kHz.



4 Quadrant Linear Stage

- Linear Regulation based on Mosfets.
- Mosfet used as
  - polarity switch in generator mode
  - programmable resistor to dissipate Magnet energy.
- Use of 4QLS as an active filter
- Use of 4QLS to pre-load inverter (continuous mode)
- Circulating current always present but value depending from load current (no mode change transition, both DCDC outputs always minimum loaded



LHC ±120A ±10V Topology Choice

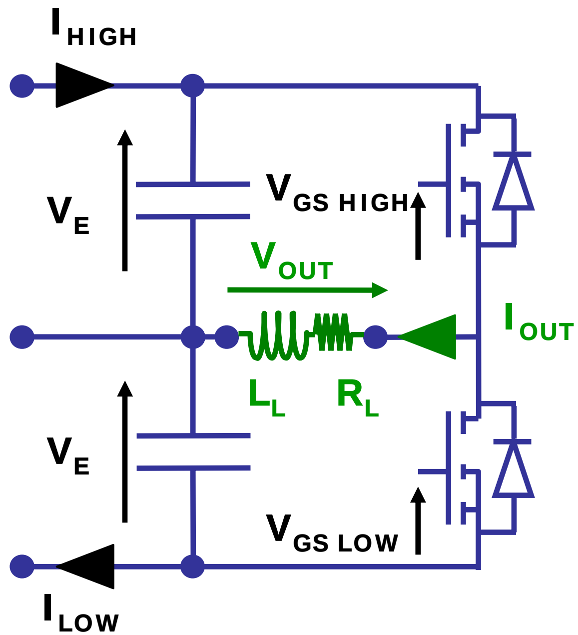
Highlights on 4QLS

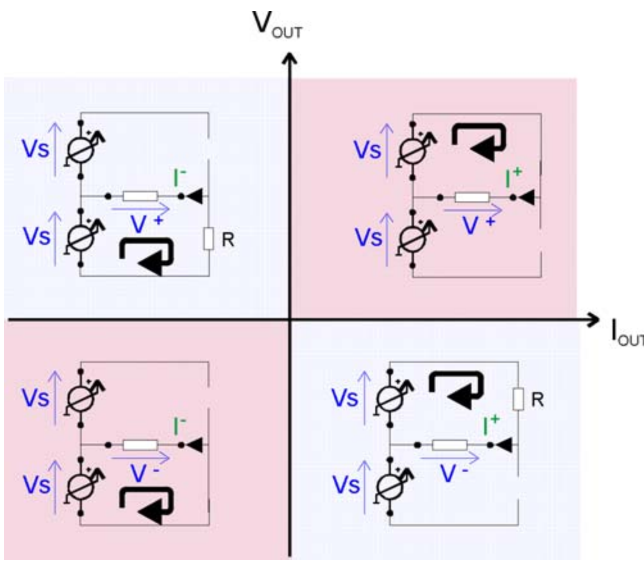
- A double power source programmable via inverter (V_E)
- 2 MOSFETS, Q1 & Q2, used as switch and programmable resistor. (high level of power possible)
- A command which works according to :

$$V_{OUT} = +(V_E - R_{HIGH} \cdot I_{HIGH})$$

$$V_{OUT} = -(V_E - R_{LOW} \cdot I_{LOW})$$

R_{HIGH} & R_{LOW} are equivalent MOSFET resistance



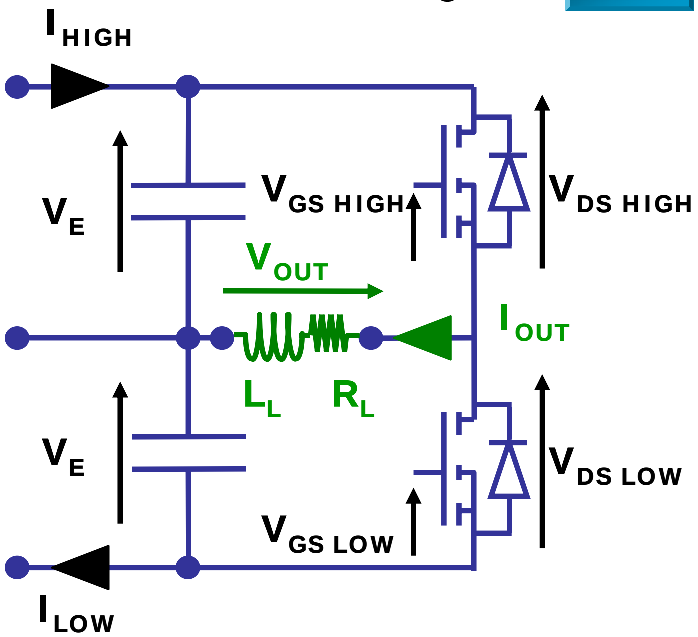


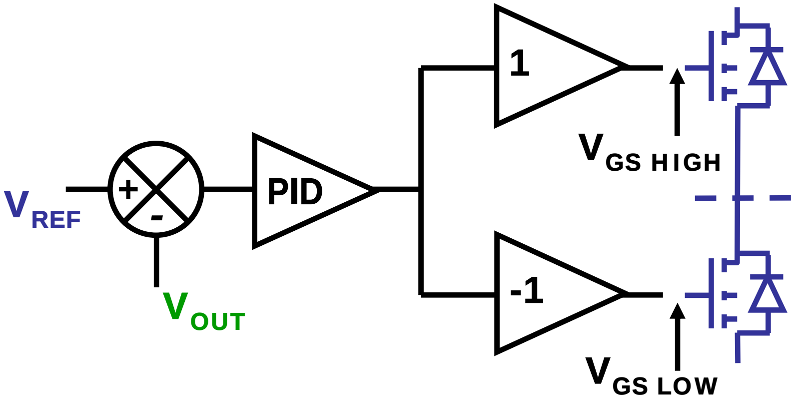
LHC: 4QLS without circulation current

- Remember a limitation of the linear stage…

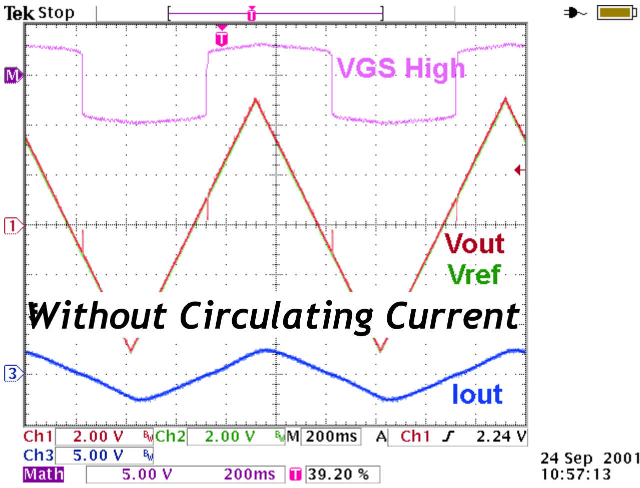
  - Main Loop (VOUT linear regulation loop) cannot provide needed step for biasing MOSFET (-3V to + 3V)

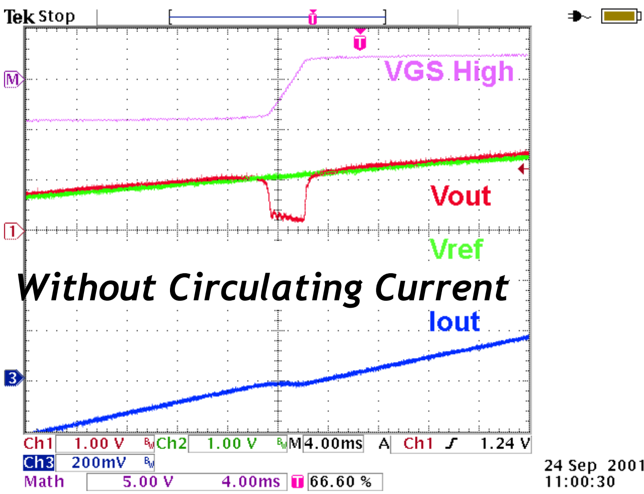
  - Playing with fixed bias is a bad idea!!! Discrepancies on $V_{GS\ ON}$ ±1V !!!





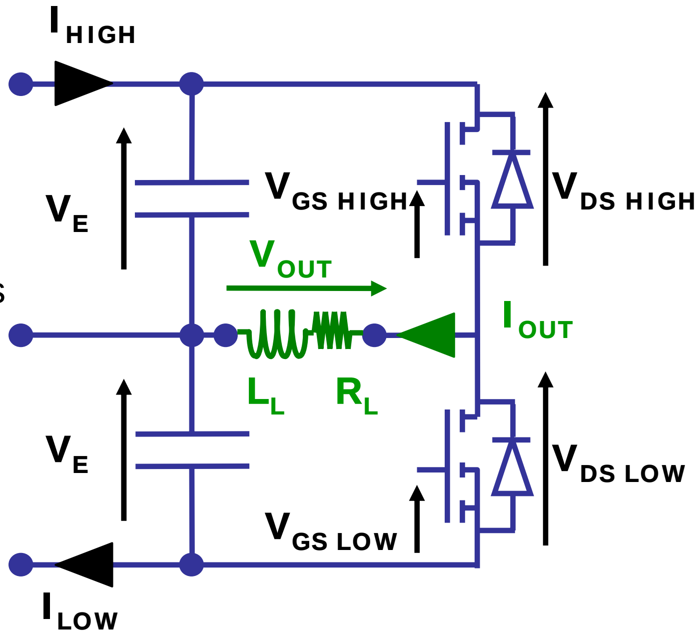
LHC ±120A ±10V Measurements

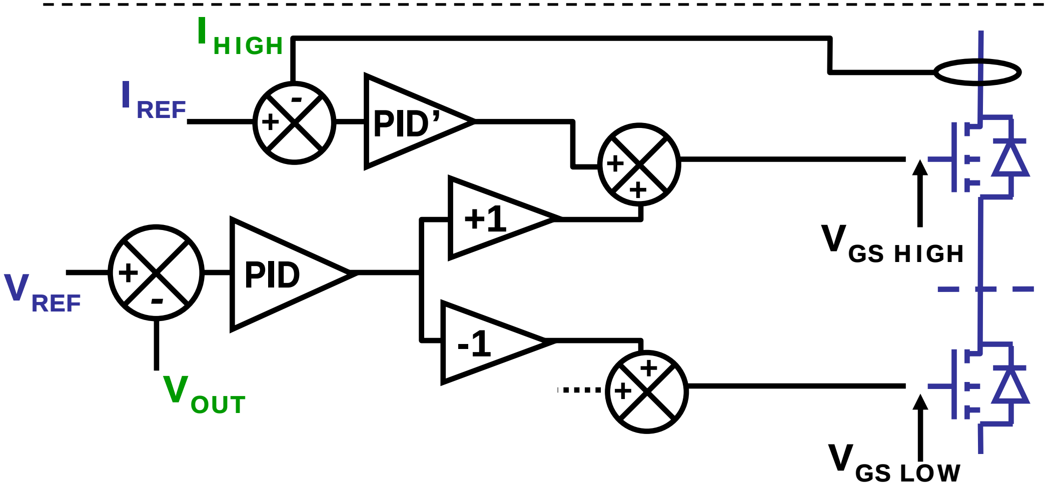




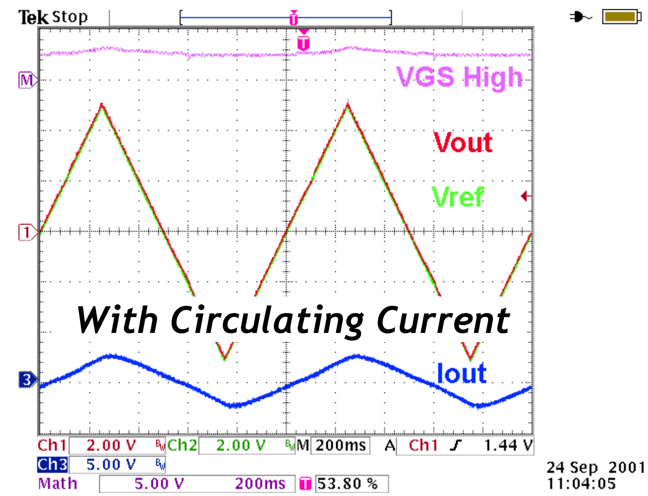
LHC: 4QLS with circulation current

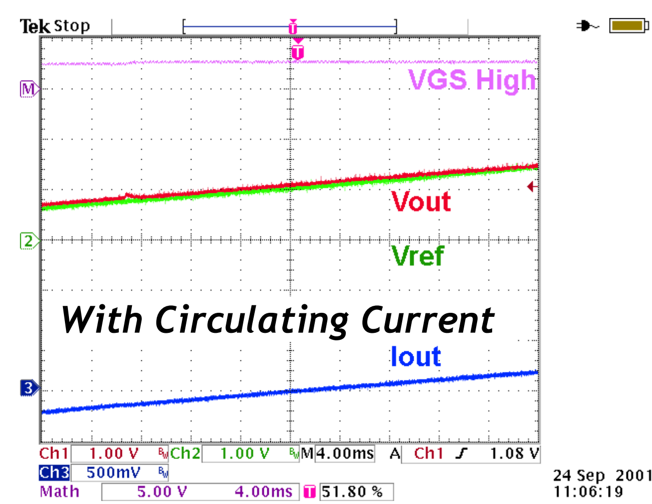
- Adding 2x circulation current loop
  - To avoid 0A distortion crossing , a circulating can help, biasing MOSFET gates.
  - These additional loops (one per MOSFET) must not perturb main loop. (must be slower)
  - $I_{Circulation}$ can vary





LHC ±120A ±10V Measurements



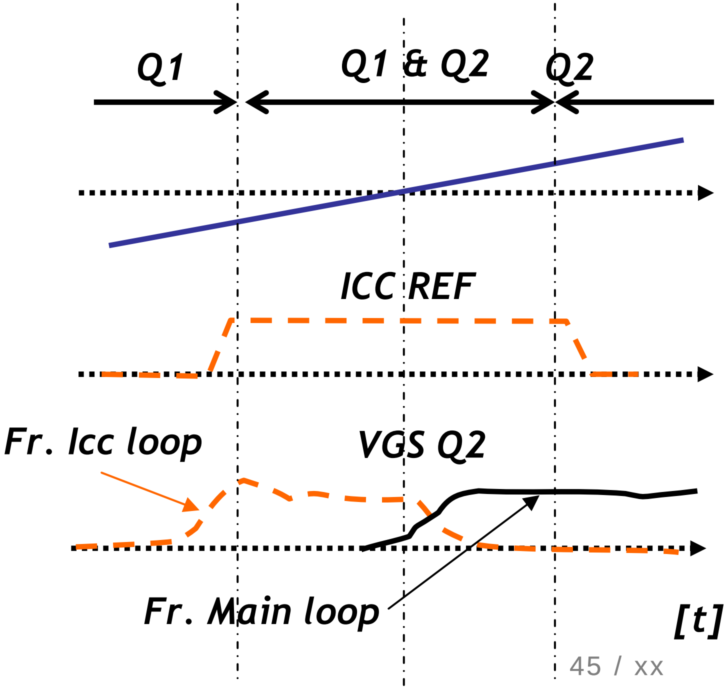


LHC: 4QLS with circulation current

different approaches:

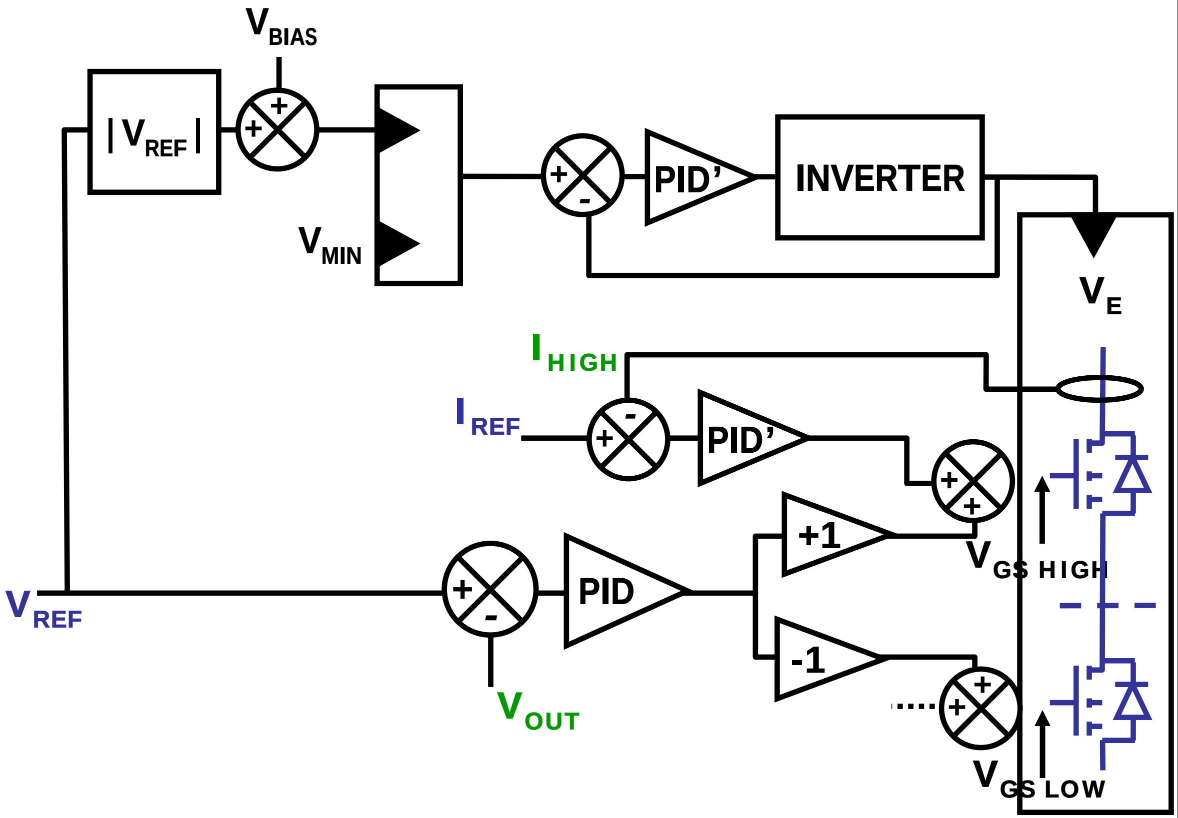
- **Circulating current always present, changing its value depending on output current**
  - Its control is easy (reference is only smoothly changing with I_{OUT})
  - Inverter reference must always be set so that this circulating current is possible leading to higher losses in receptor mode.
  - No changing mode (Gate of each side MOSFET always biased)

- **Circulating current only present when close to a potential transition**
  - This solution saves a lot of energy when recovering, since inverter doesn't inject power in MOSFET when absorbing power.
  - dI/dt Limitation exists, since if too fast, circulating current doesn't have time to appear and MOSFET Gate are not well biased.

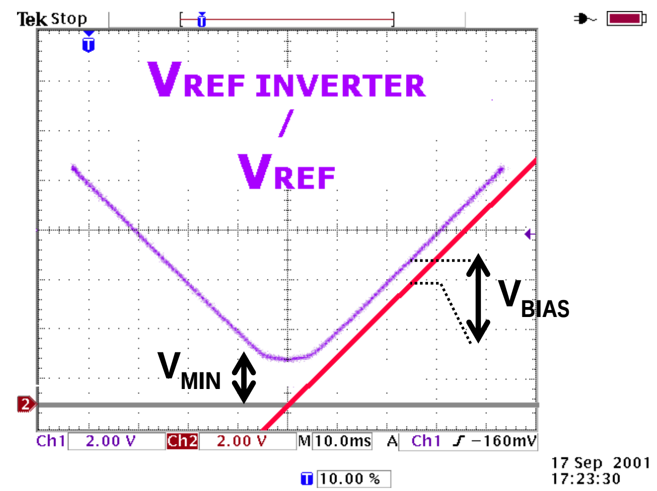


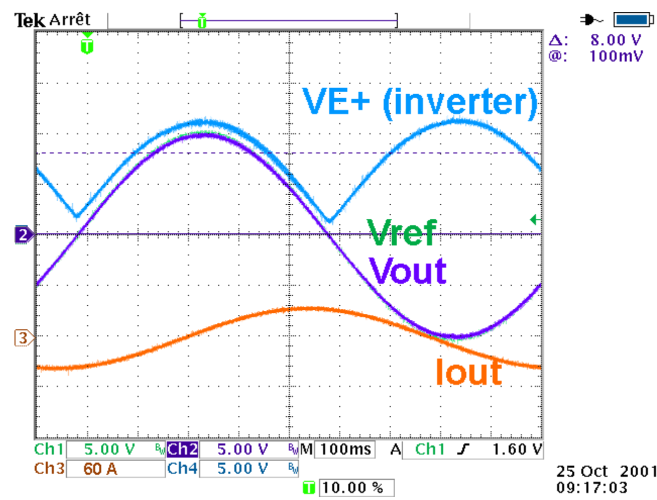
LHC: 4QLS / Inverter Reference

- Inverter REF is built according to
  - VBIAS MIN. not to saturate MOSFET (i.e saturate Loop)
  - VBIAS OPT. For 4Q Linear stage acting as active filter (better rejection of mains disturbances and 300 Hz)
  - VMIN coupled to I circulation MIN to always minimum load inverter (Conduction mode un-changed)
  - Inverter Loop must be faster / transparent than 4Q stage loop



LHC ±120A ±10V Measurements





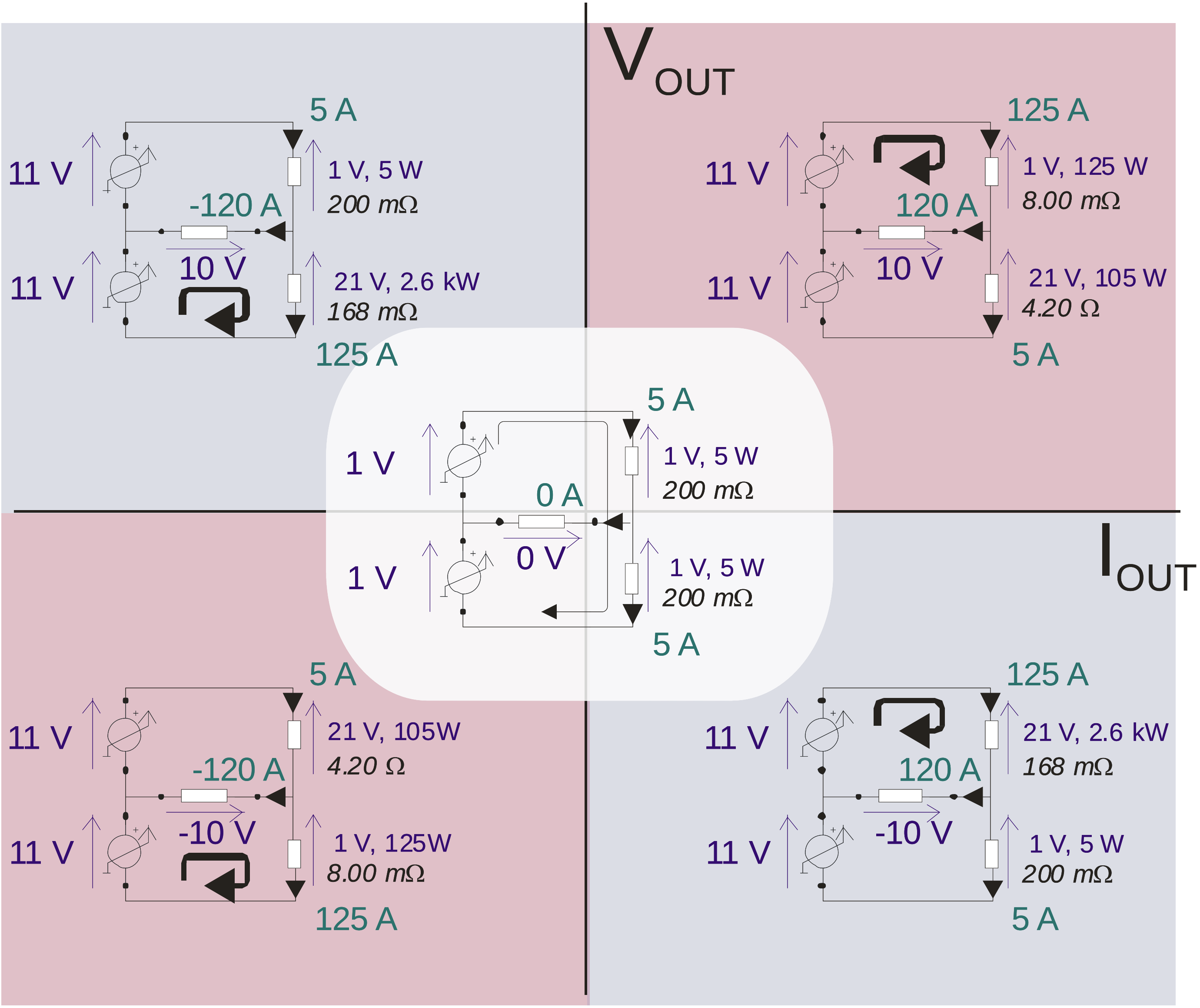
LHC: 4QLS MOS working Area (Example)

Practical case of Circulation current always ON, at the same value: 5A.

RDSON variations limited by circulating current.

Dissipate Power is:

- *21V x 120A in recovering MOSFET instead of 10V x 120A required by the load.*
- *Only valid if not often the case.*



LHC: 4QLS MOS Model (FB180SA10 I.R.)

MOSFET is difficult to control directly from the main loop to the gate. Indeed gain is from virtually 0 if saturated to thousands when almost OFF.

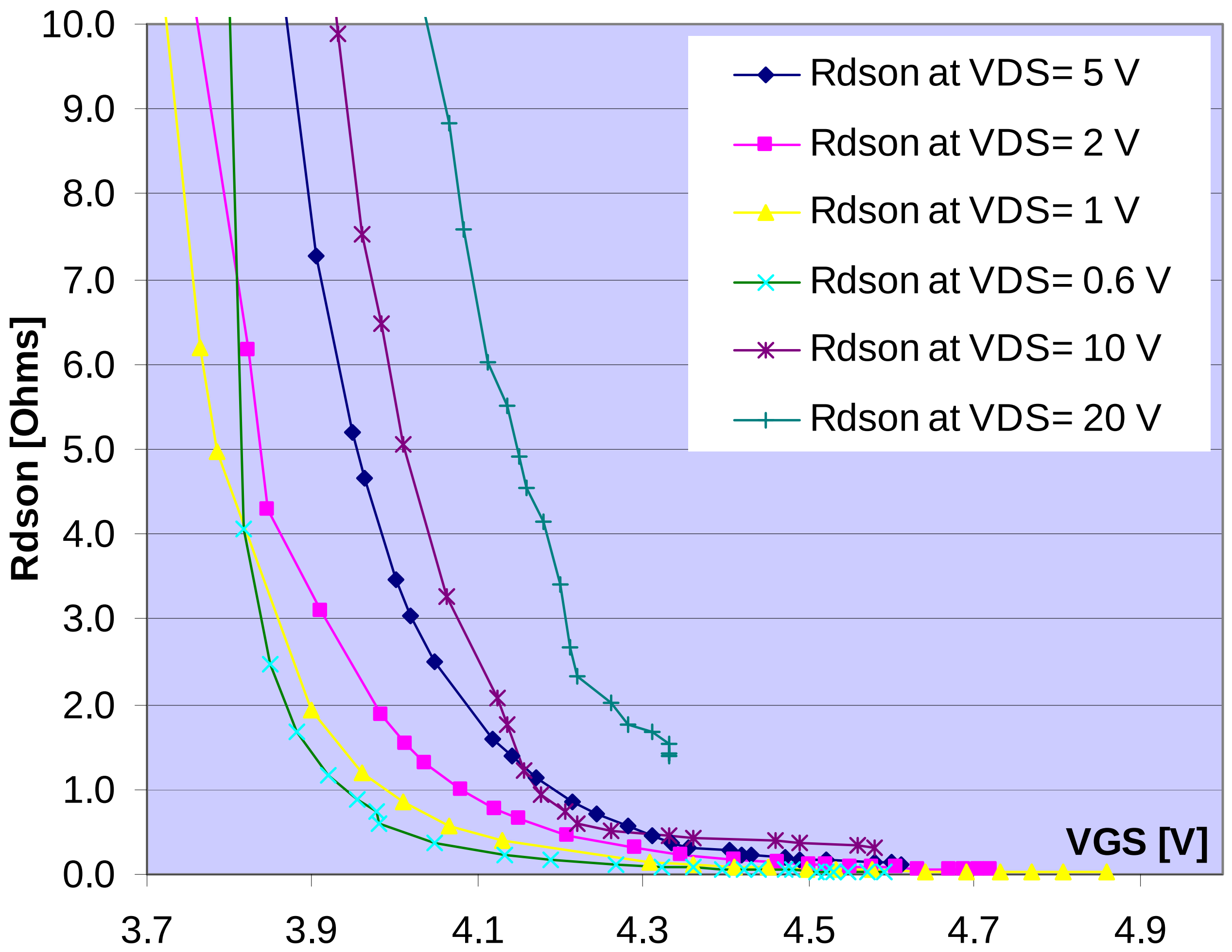
Settings like:

- Circulating current value

- Difference voltage issued from the inverter output voltage

- Number of MOSFET in //

are the key to maintain a stable efficient analog loop.



LHC: Practical Results

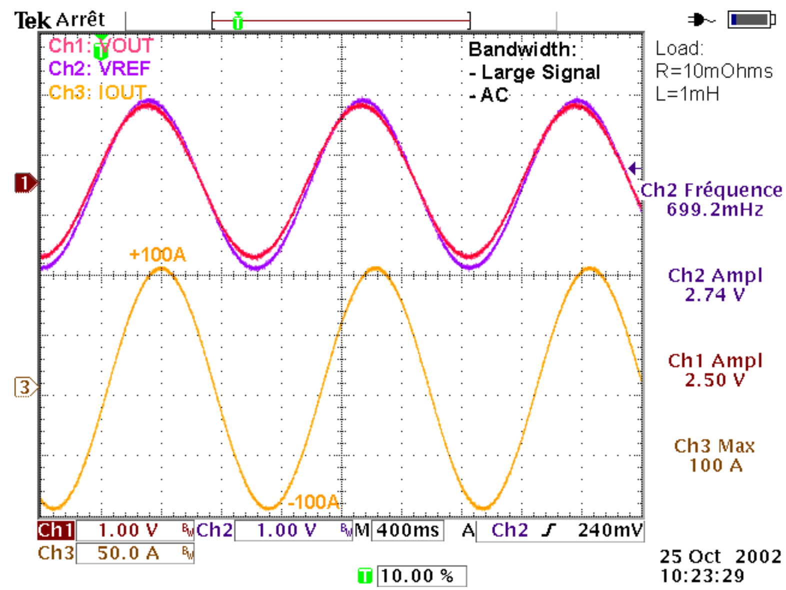
DISTORTION ?:

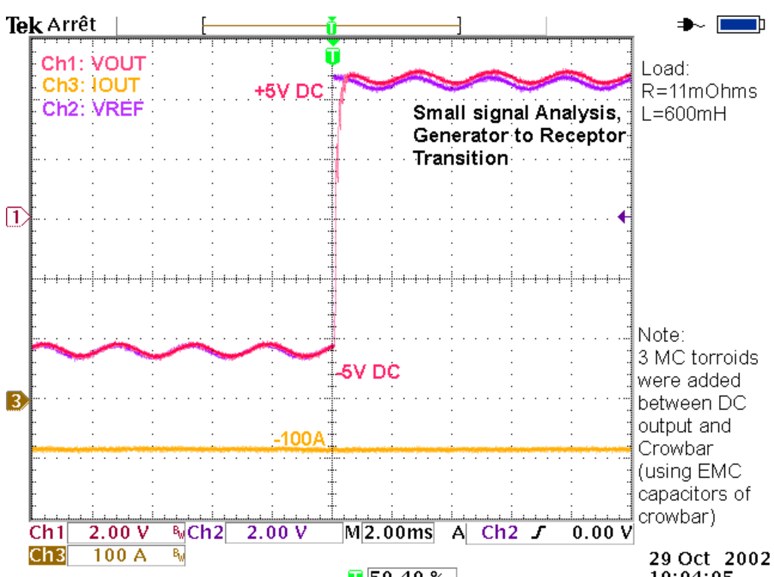
Crossing axis is OK. No distortion, achieved thanks to circulating current.

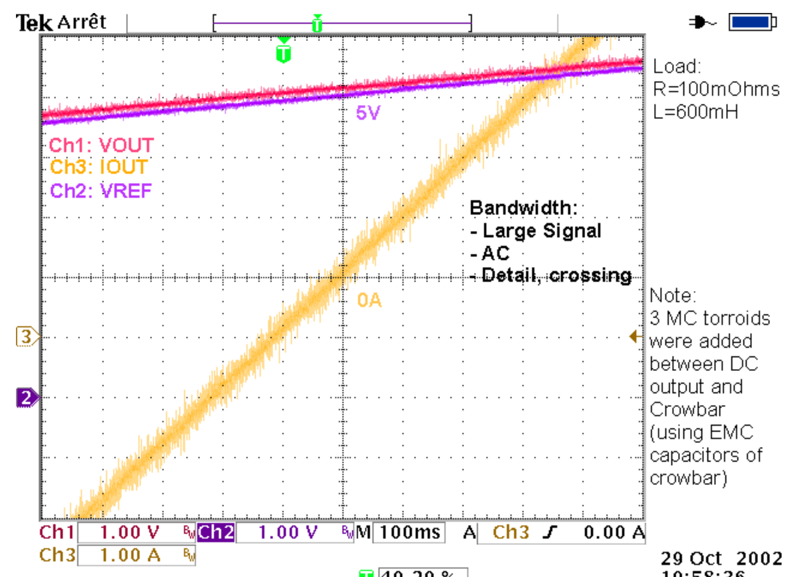
CONTROL:

Bandwidth in generator & receptor quadrant
Crossing 0A is OK, being unchanged.

LHC ±120A ±10V Measurements







LHC: Realizations

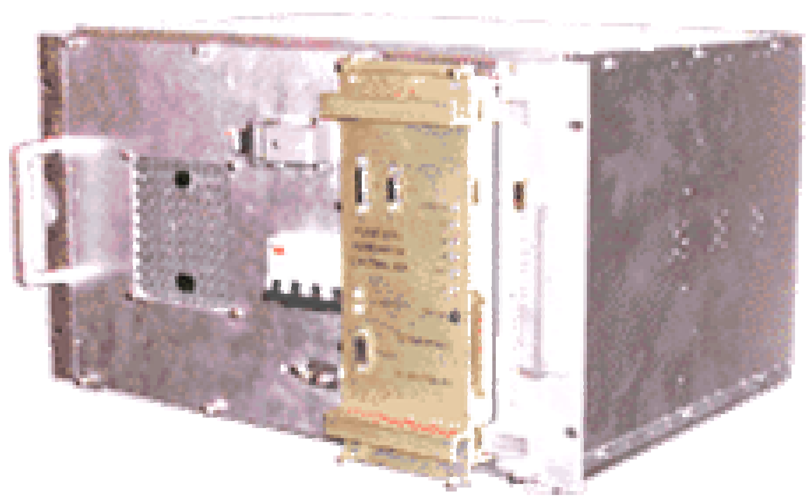
LHC ±120A ±10V

- 330 Converters
- Correctors
- CERN Internal Design

CERN / EFACEC / CEL

LHC ±60A ±8V

- 800 Converters
- Orbit Correctors
- Below Dipoles, in a radiation zone
- CERN Internal Design



CIRTEM

LHC ±600A ±10V

- **440 Converters**
- **1x 6U Module**

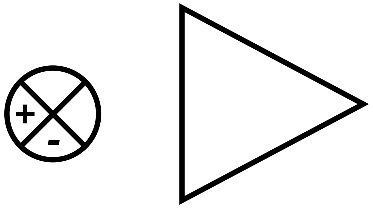
TRANSTECHNIK

LHC ±600A ±40V

- **50 Converters**
- **2x 6U module**

Thank you for your attention.

AND?...END.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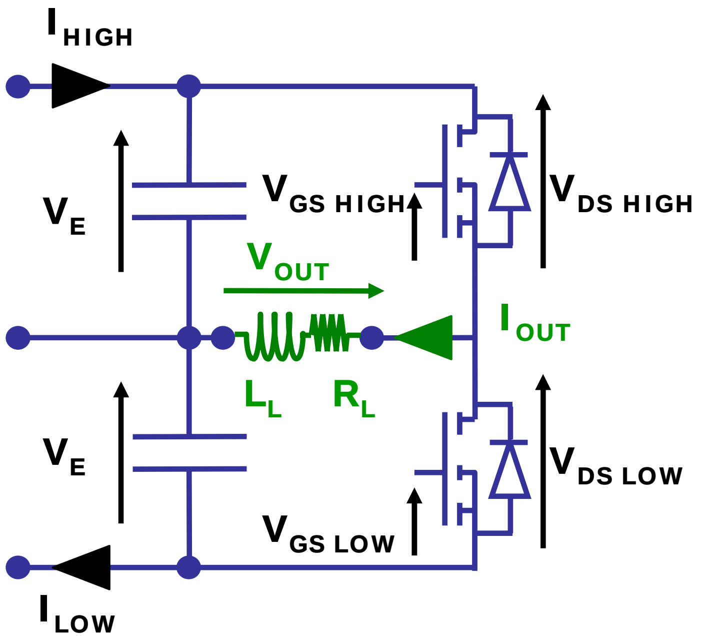
I HIGH
V E
V E
V GS HIGH
V DS HIGH
V OUT
I OUT
L L
R L
V DS LOW
V GS LOW
I LOW

Reference

Care with test invisble so that alignment is ok