Analog digital conversion

(in beam instrumentation systems)

Marek Gasior

CERN Beam Instrumentation Group

BI CAS 2018, Tuusula, Finland

Introduction

- One hour lecture for the topic described in many thick books and lectured at universities over months
- More standard topic than for most of other lectures
- Focus on aspects important in beam instrumentation
- What should I take into consideration while choosing an ADC for my system ?

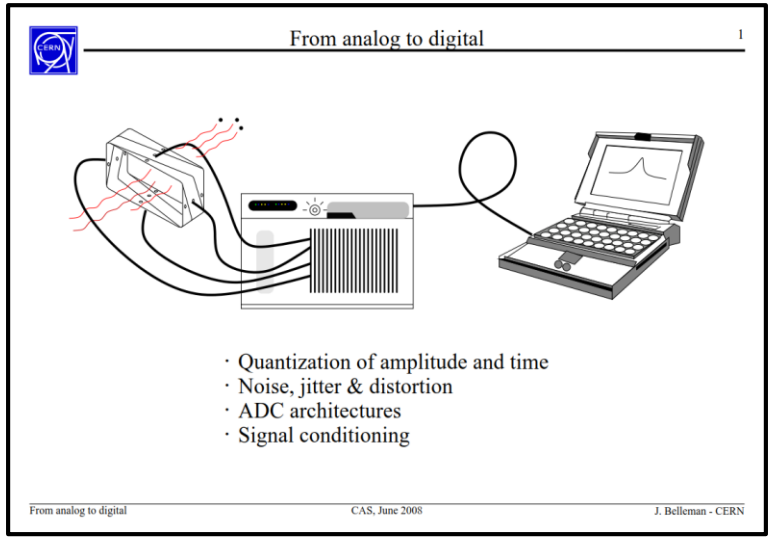
Outline:

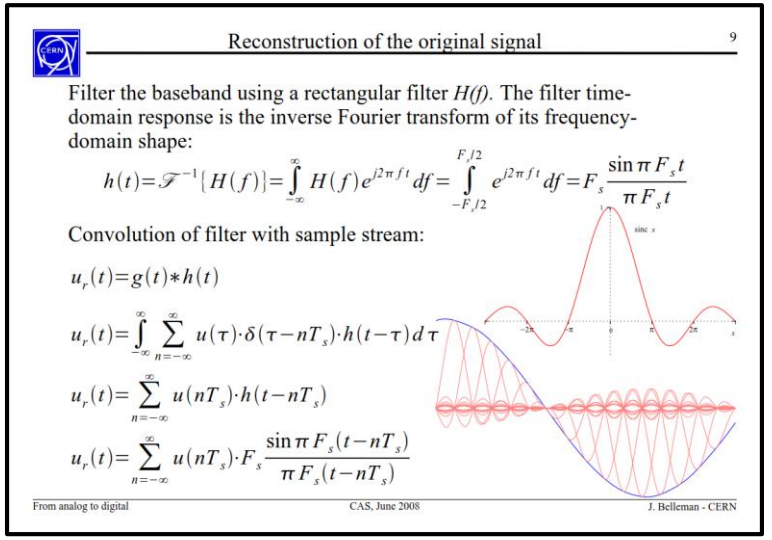
- ADC fundamentals
- Which sampling rate do I need ?
- How many bits do I need ?
- A glance on three datasheets
- A few examples of ADC modules

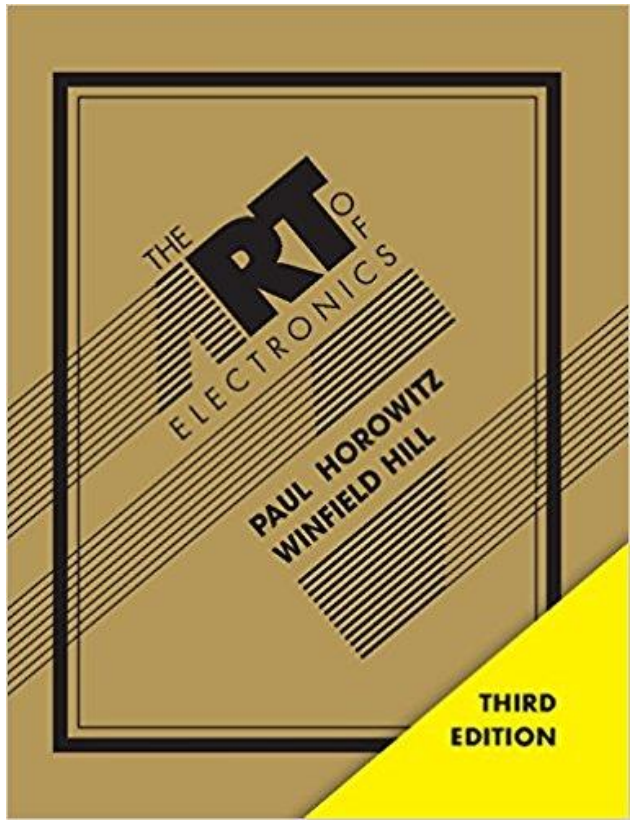
Literature

- "From analog to digital" by Jeroen Belleman
  - two hour lecture during CAS 2008 in Dourdan
  - lecture: http://cas.web.cern.ch/files/lectures/dourdan-2008/belleman.pdf
  - paper (pages 281 – 316): http://cdsweb.cern.ch/record/1071486/files/cern-2009-005.pdf

- "Art of Electronics, 3rd edition", P. Horowitz, W. Hill
  - Chapter 13: "Digital meets analog", pages 879 – 955
  - Excellent book
  - For everybody, beginners and experts

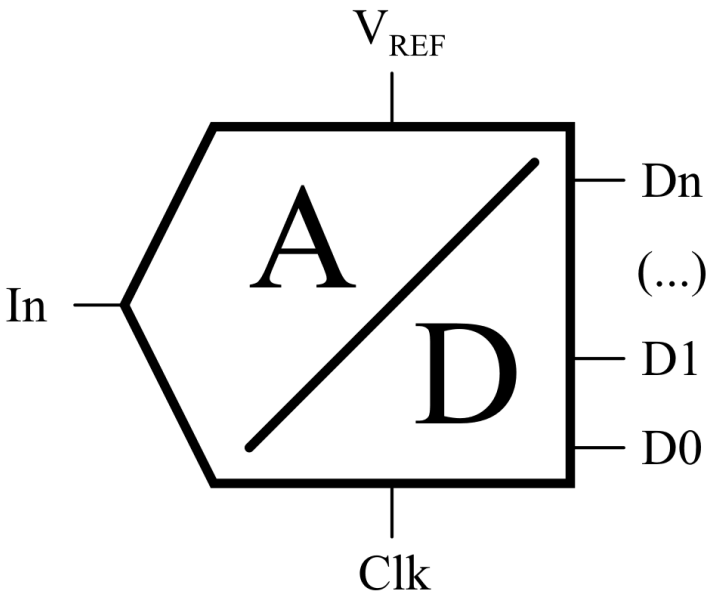




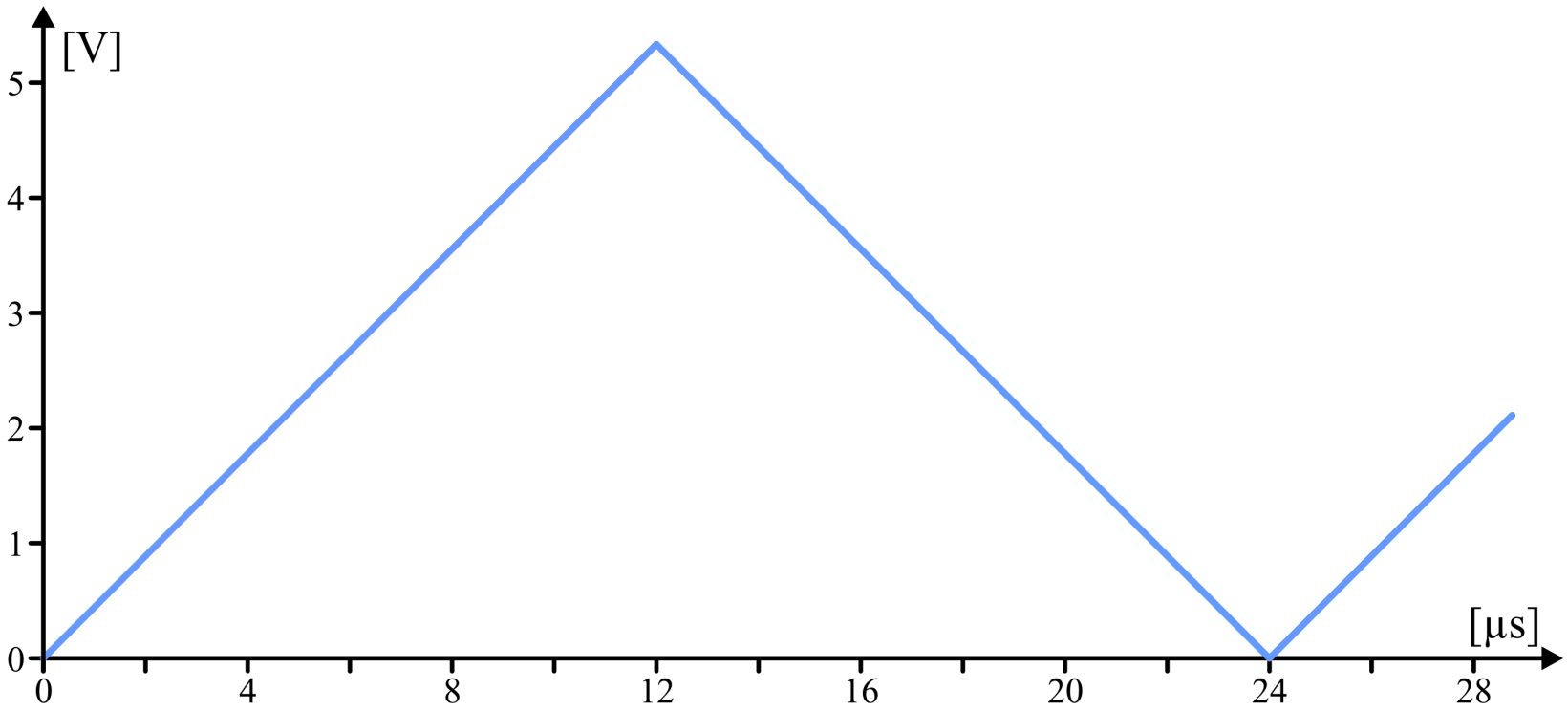


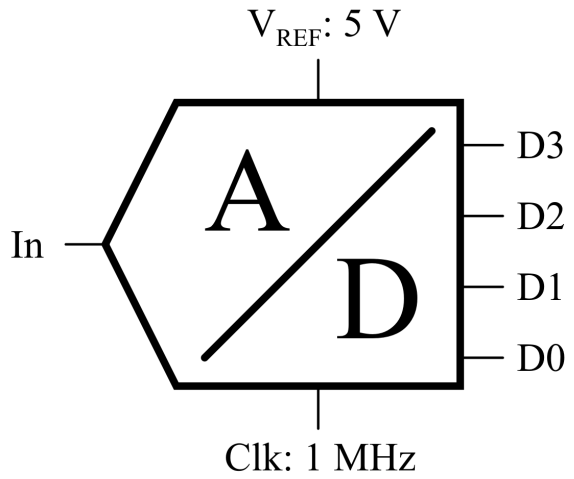
Why ADCs ? What is an ADC ?

- Beam instrumentation signals (voltages, currents, light, …) are analog and the control room is “numeric”
- Processing of numbers is by far more powerful than processing of analog signals
- ADCs are very important parts of BI systems and often put a limit for the system performance
- An ADC is an electronic circuit which converts an analog signal (continuous time, continuous amplitude) into a digital signal (discrete time, discrete amplitude = series of pairs of numbers)
- An ADC is an integrated circuit (except very special cases)
- Unfortunately an ADC chip does not work alone
- Digital data must be taken and send further

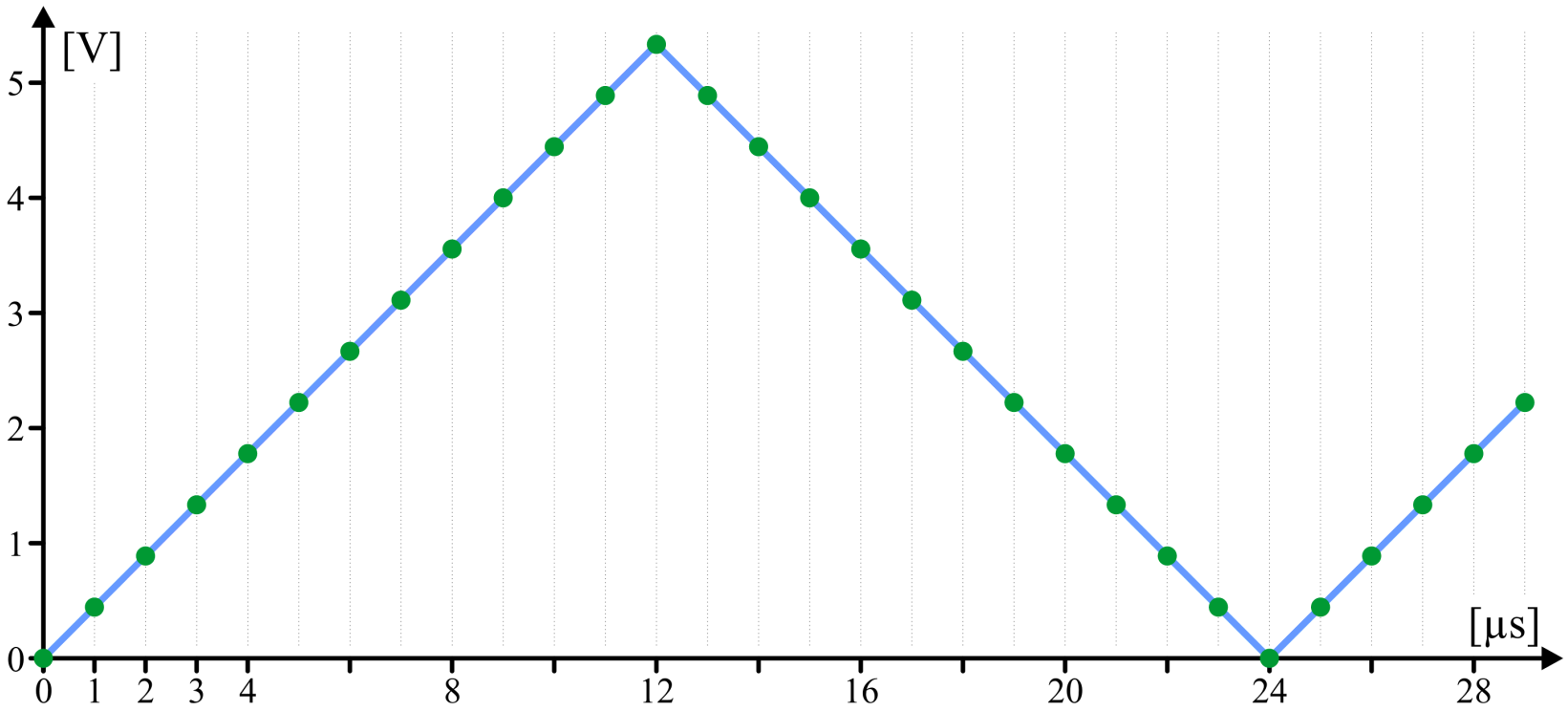


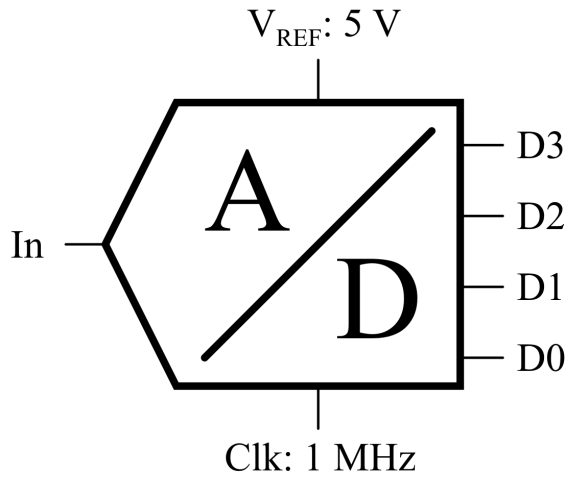
Sampling



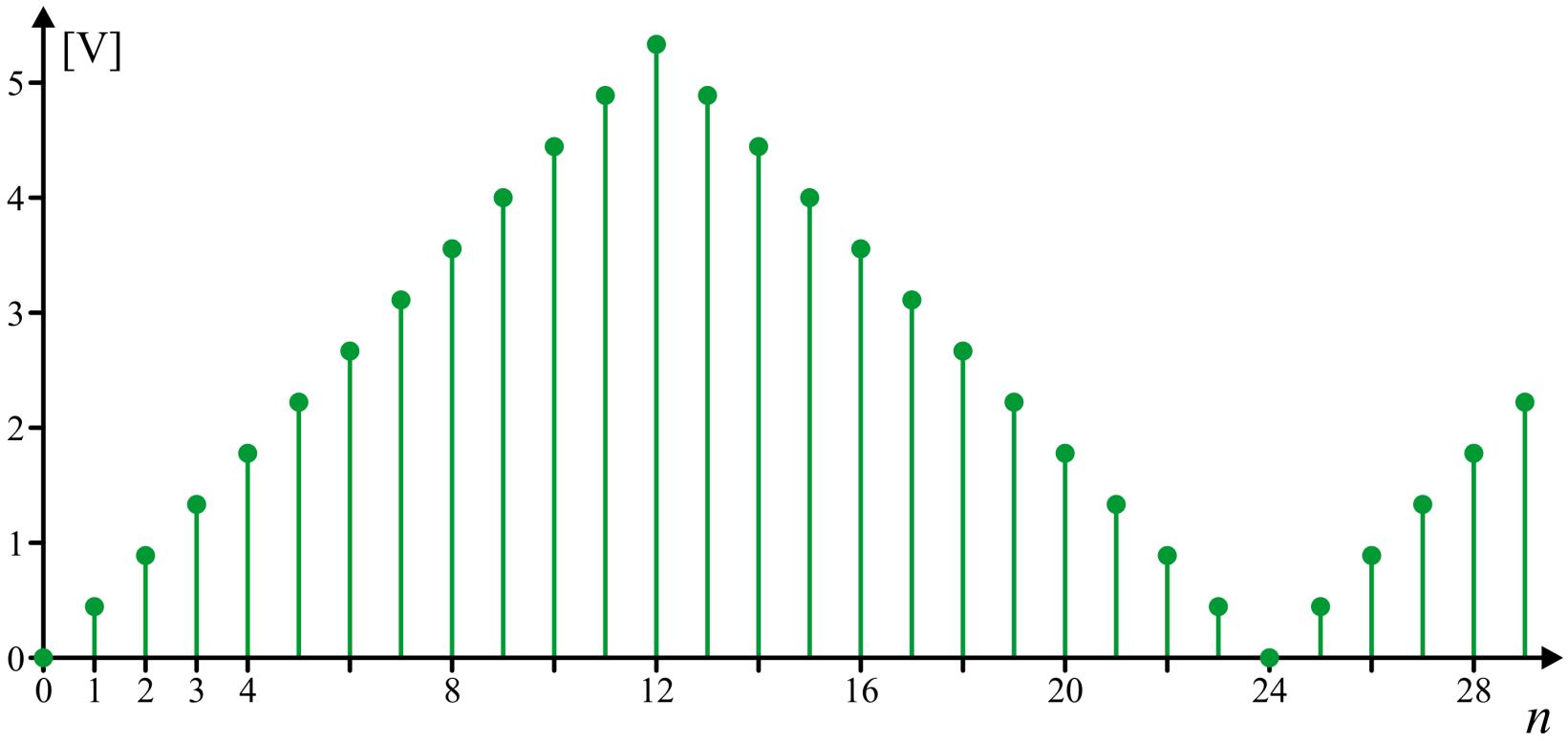


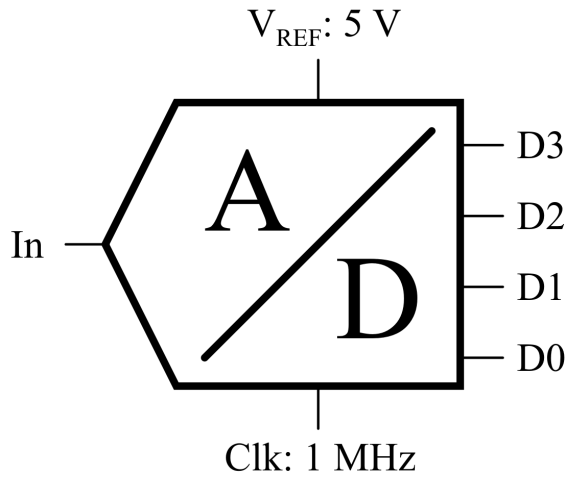
Sampling


[V]
5
4
3
2
1
0
0
1
2
3
4
8
12
16
20
24
28
[µs]

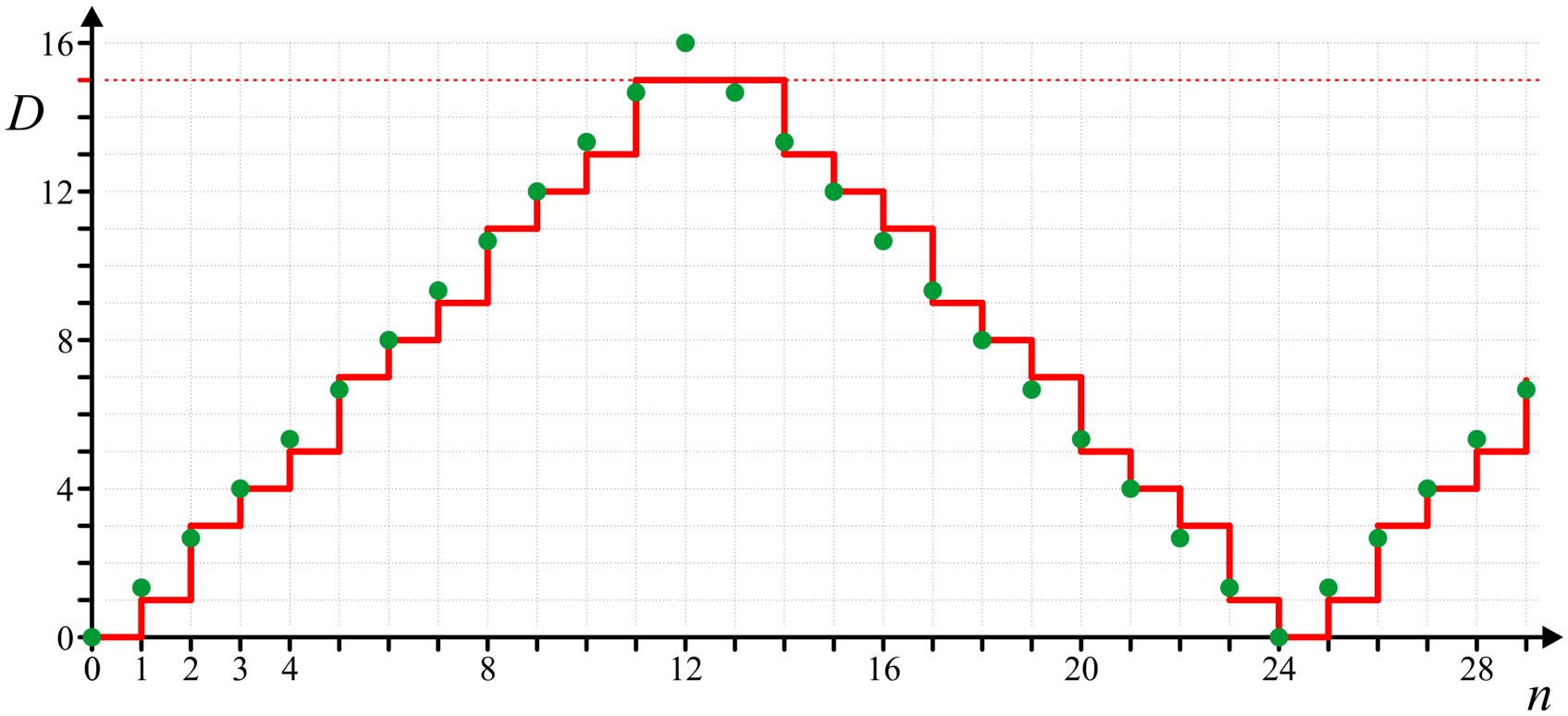

V_{REF}: 5 V
A
D
In
D3
D2
D1
D0
Clk: 1 MHz

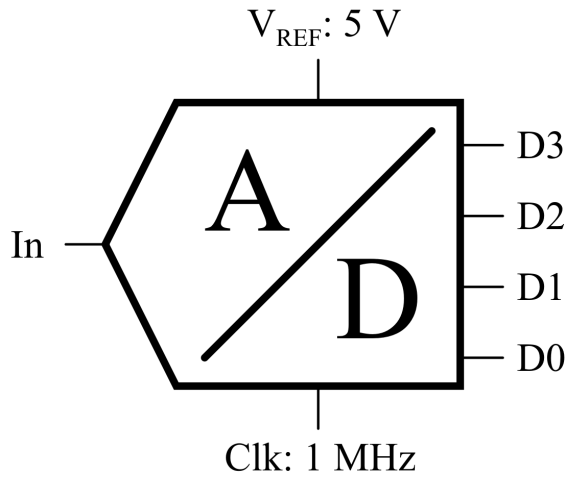
Sampling



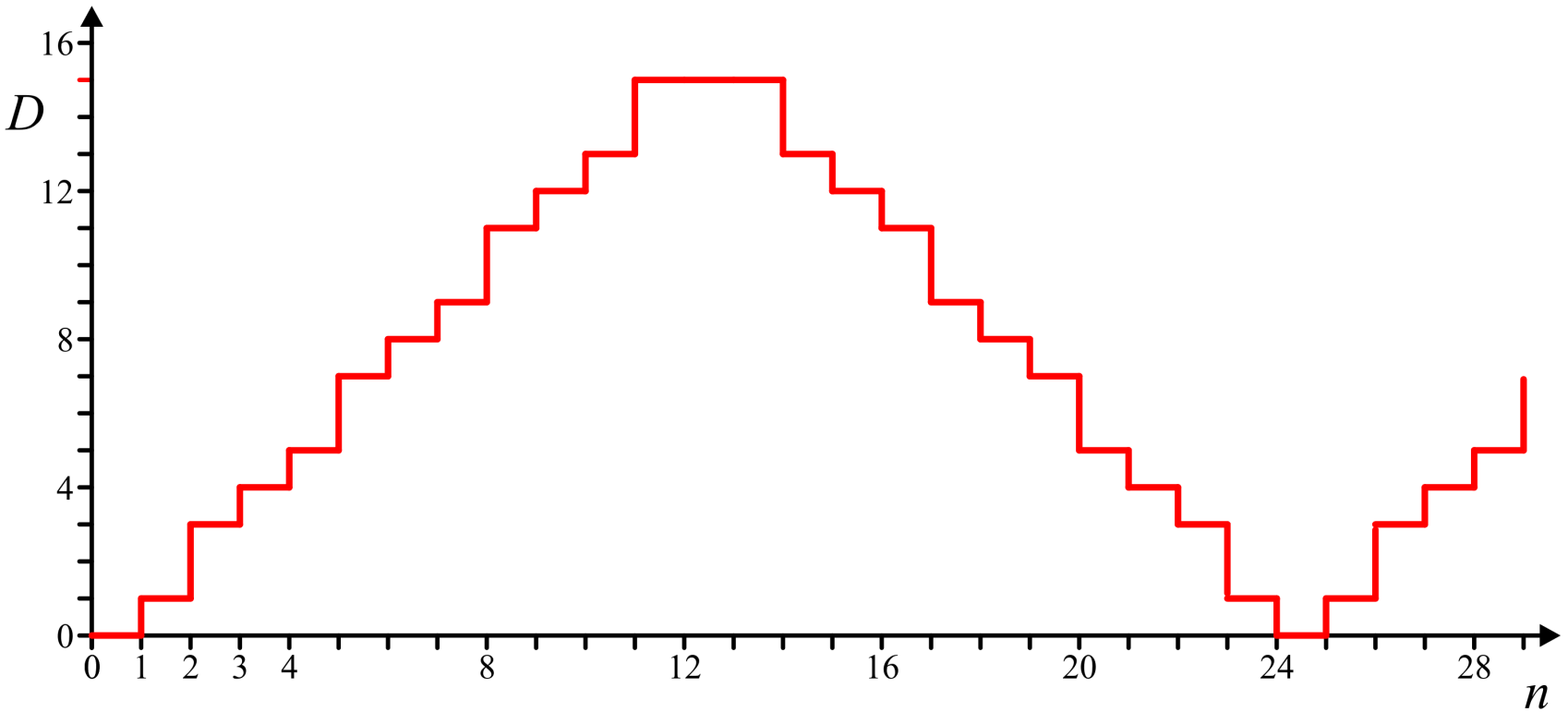


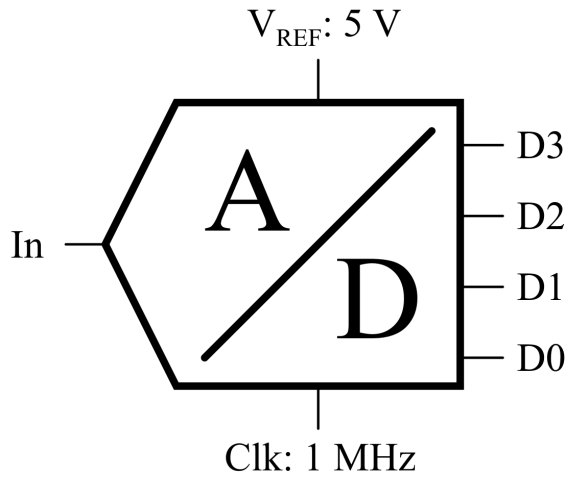
Sampling and quantization





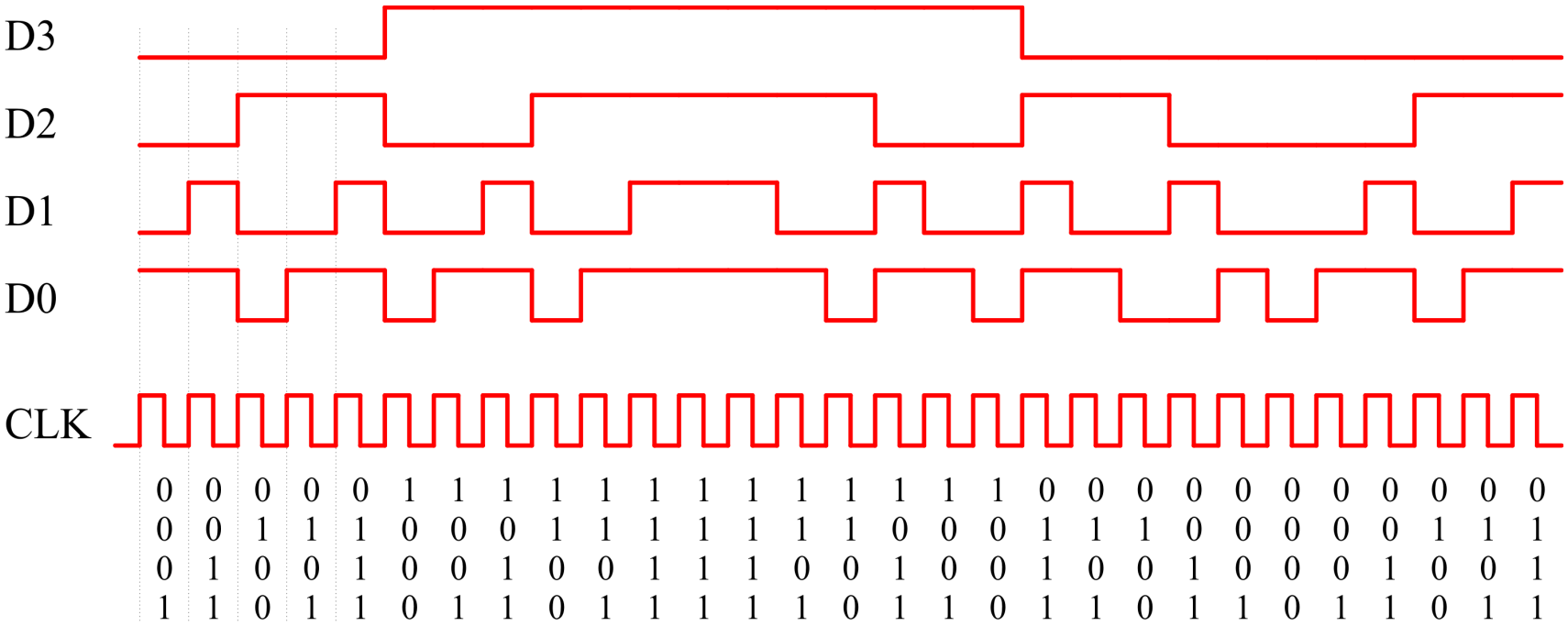
Sampling and quantization





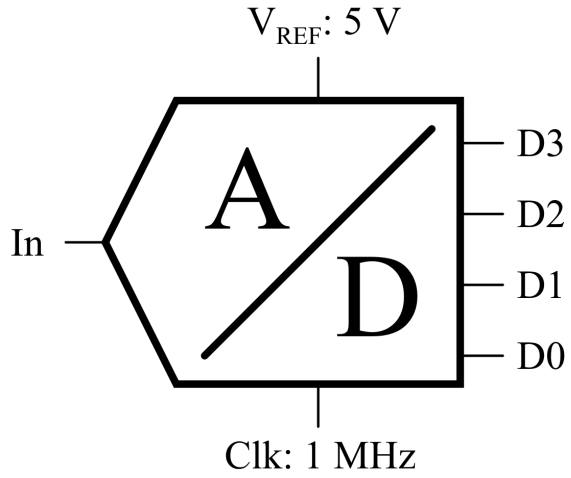
D	1	3	4	5	7	8	9	11	12	13	15	15	15	13	12	11	9	8	7	5	4	3	1	0	1	3	4	5	7
n	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29

Sampling and quantization

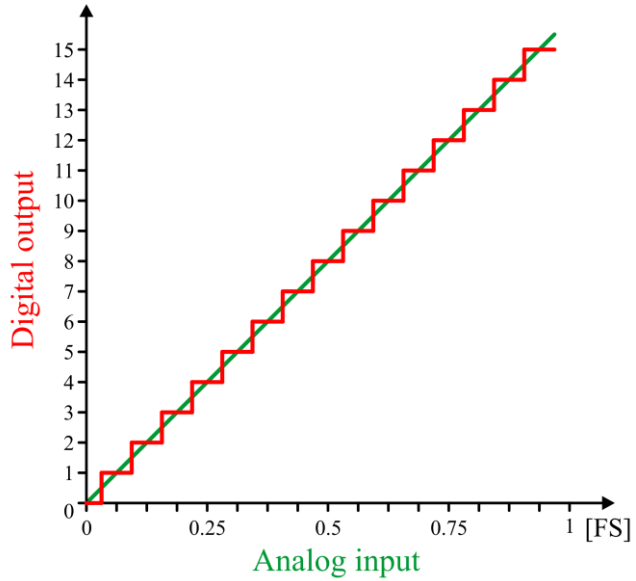


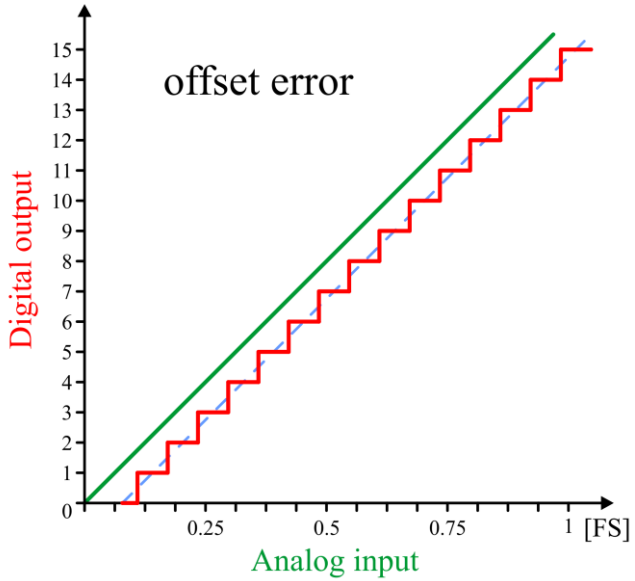
	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	0	0	1	1	1	0	0	0	1	1	1	1	1	1	1	0	0	0	1	1	1	0	0	0	0	0	1	1	1
	0	1	0	0	1	0	0	1	0	0	1	1	1	0	0	1	0	0	1	0	0	1	0	0	0	1	0	0	1
	1	1	0	1	1	0	1	1	0	1	1	1	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1

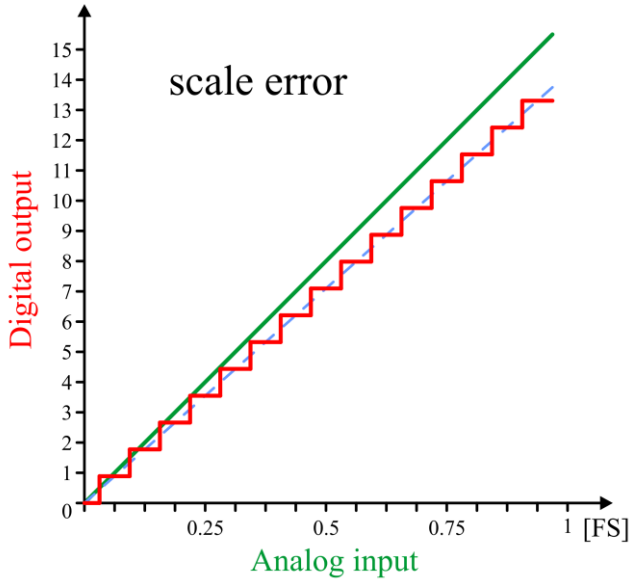
D	1	3	4	5	7	8	9	11	12	13	15	15	15	13	12	11	9	8	7	5	4	3	1	0	1	3	4	5	7
n	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29

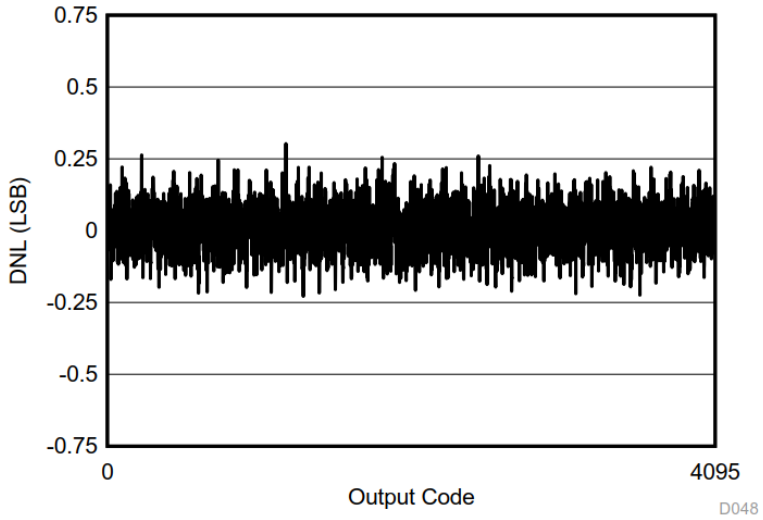


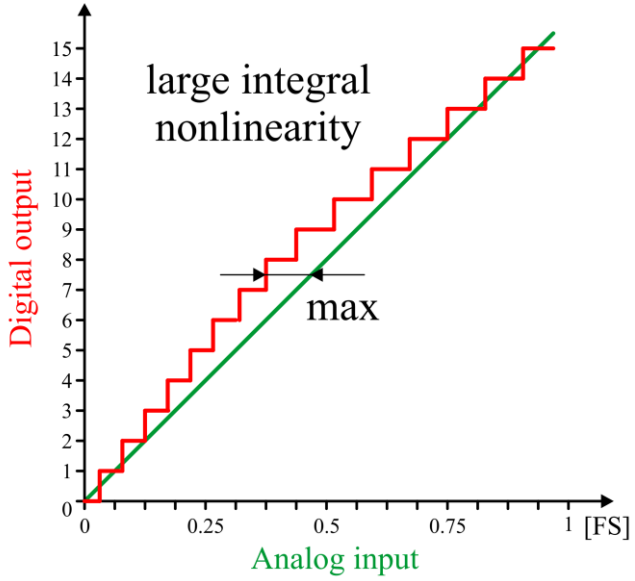
ADC errors

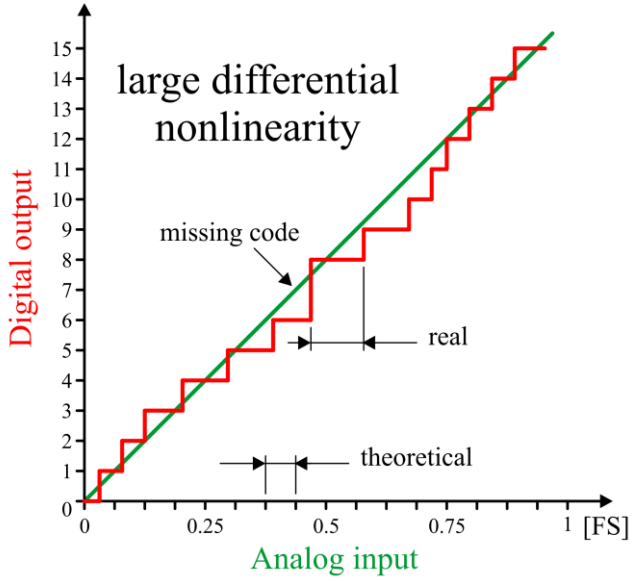

Digital output
Analog input
0
0.25
0.5
0.75
1 [FS]


offset error
Digital output
Analog input
0
0.25
0.5
0.75
1 [FS]


scale error
Digital output
Analog input
0
0.25
0.5
0.75
1 [FS]

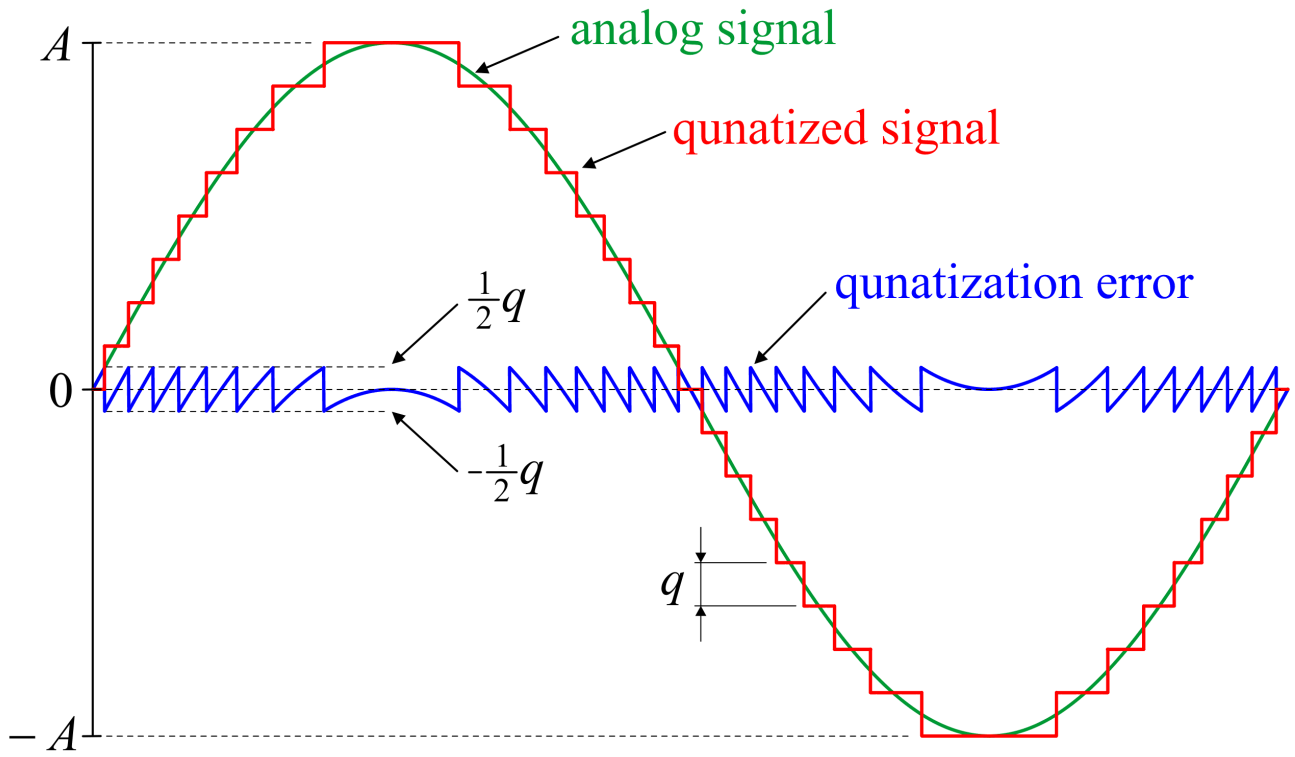

DNL (LSB)
0.75
0.5
0.25
0
-0.25
-0.5
-0.75
0
4095
Output Code
D048


large integral
nonlinearity
max
Digital output
Analog input
0
0.25
0.5
0.75
1 [FS]


large differential
nonlinearity
missing code
real
theoretical
Digital output
Analog input
0
0.25
0.5
0.75
1 [FS]

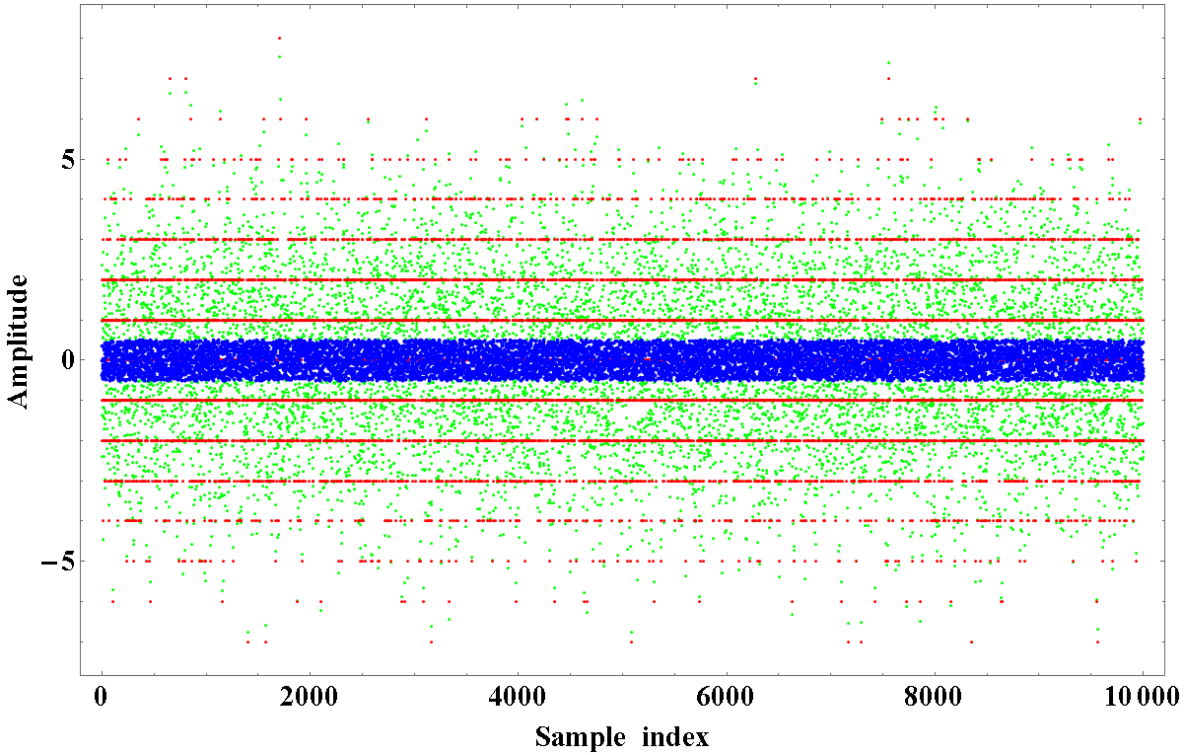
Quantization error

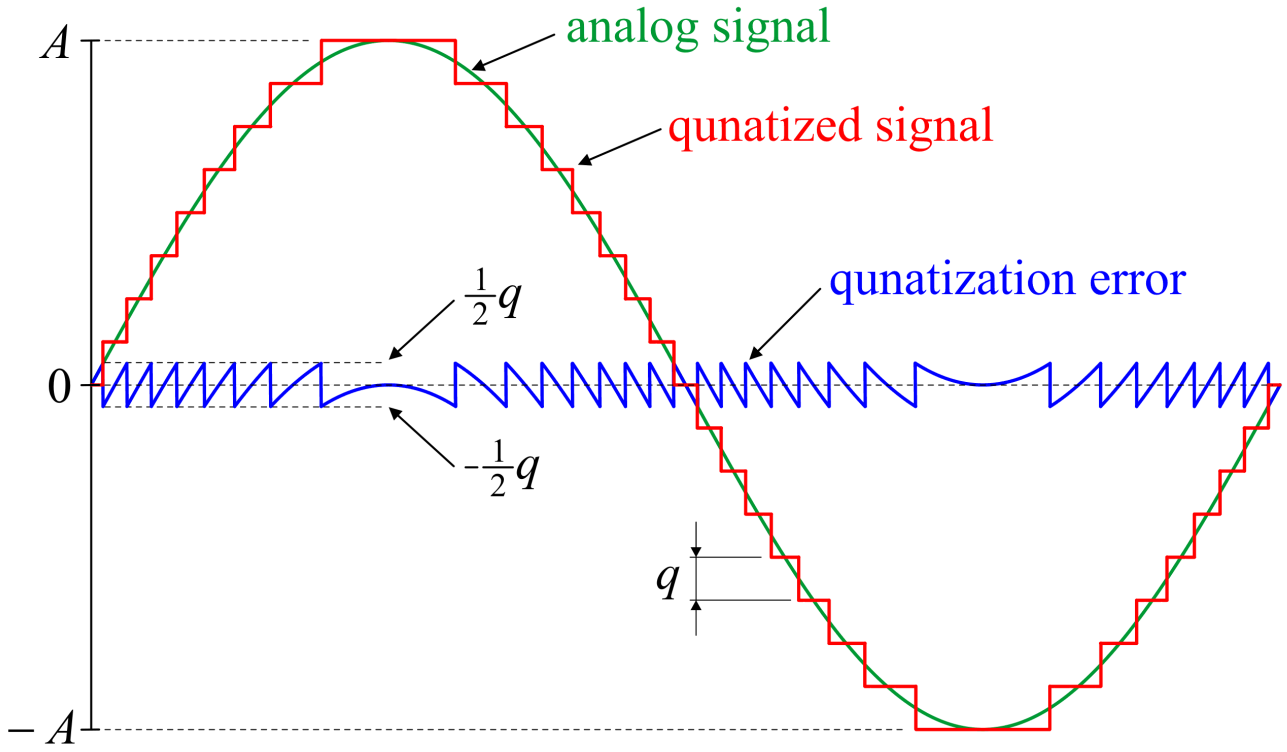
- Here we consider only an ideal quantization of a continuous signal (no sampling). Quantized signal is an approximation o the input signal; their difference is the quantization noise.
- Used quantities:
  - *A* – input signal amplitude
  - *n* – number of bits
  - *q* – one bit amplitude: $q = \frac{2A}{2^n}$



- Max quantization error: $e_m = \frac{\pm q}{2}$
- RMS amplitude of the input signal: $A_{RMS} = \frac{A}{\sqrt{2}}$
- Quantisation error RMS amplitude: $e_{RMS} = \frac{1}{\sqrt{12}} q \cong 0.289\, q$
- Signal to Noise Ratio: $SNR = \frac{A_{RMS}}{e_{RMS}} = \frac{\sqrt{6}}{2} 2^n$ $\quad SNR\ [\mathrm{dB}] = 20 \log_{10} \frac{\sqrt{6}}{2} 2^n \cong 1.76 + 6.02\, n$
- Effective Number of Bits: $ENOB = \frac{SNR\ [\mathrm{dB}] - 1.76}{6.02}$ $\quad ENOB' = \frac{SINAD\ [\mathrm{dB}] - 1.76}{6.02}$

Quantization error



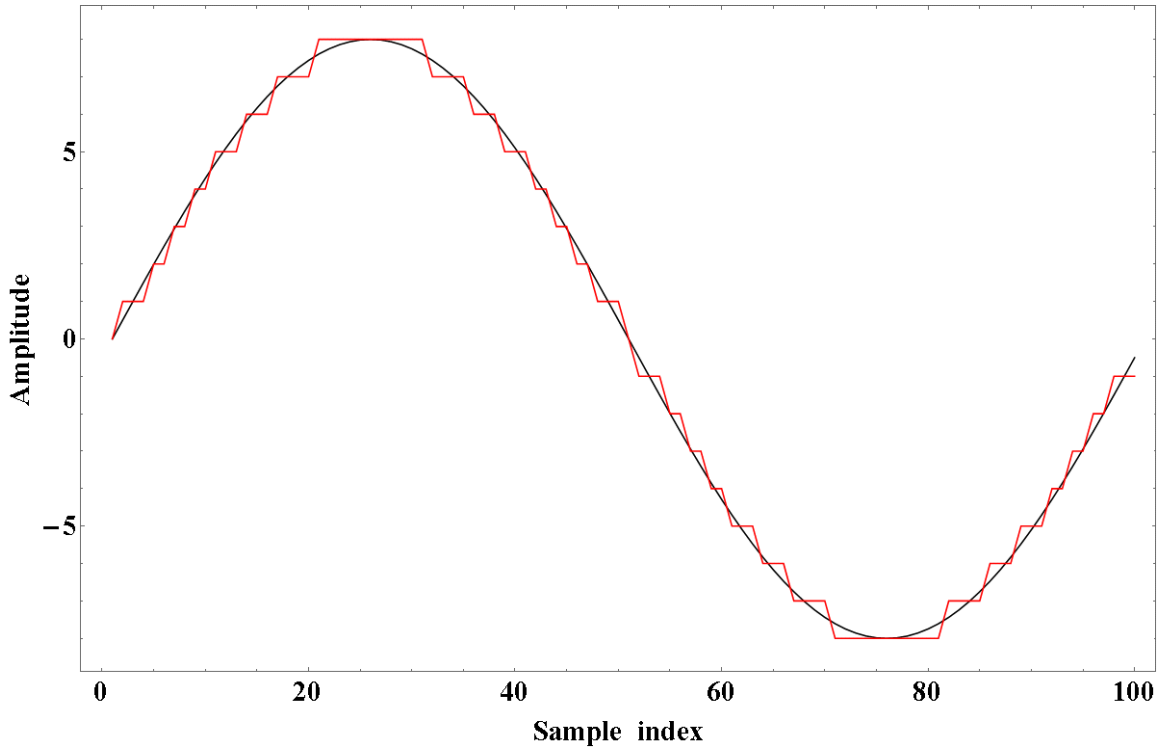


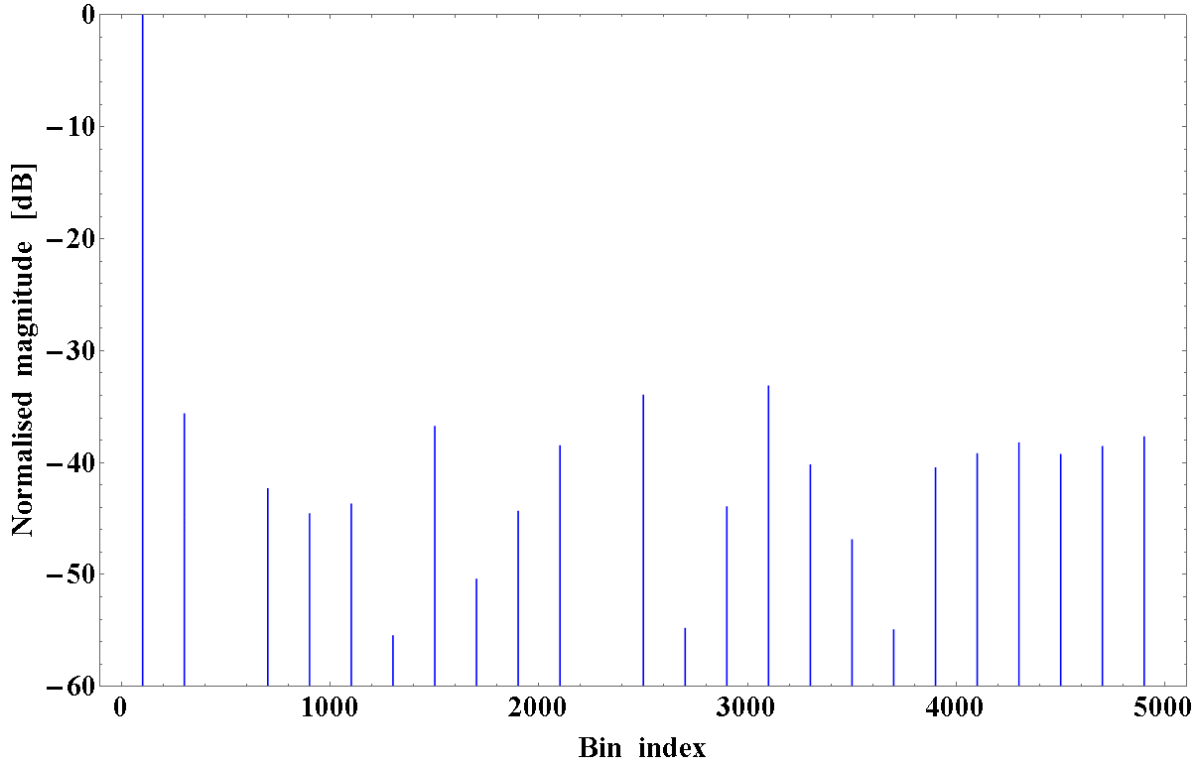
- Numerical simulation with noise as the analog input signal
- Quantization simulated with round()
- Same color coding as the “sine example”
- Now $e_{RMS} = 0.287$

$$e_{RMS} = \frac{1}{\sqrt{12}} q \cong 0.289q$$

- For numerical simulation with $n = 4$ (figure above) one gets $e_{RMS} = 0.271\ q$

Quantization error

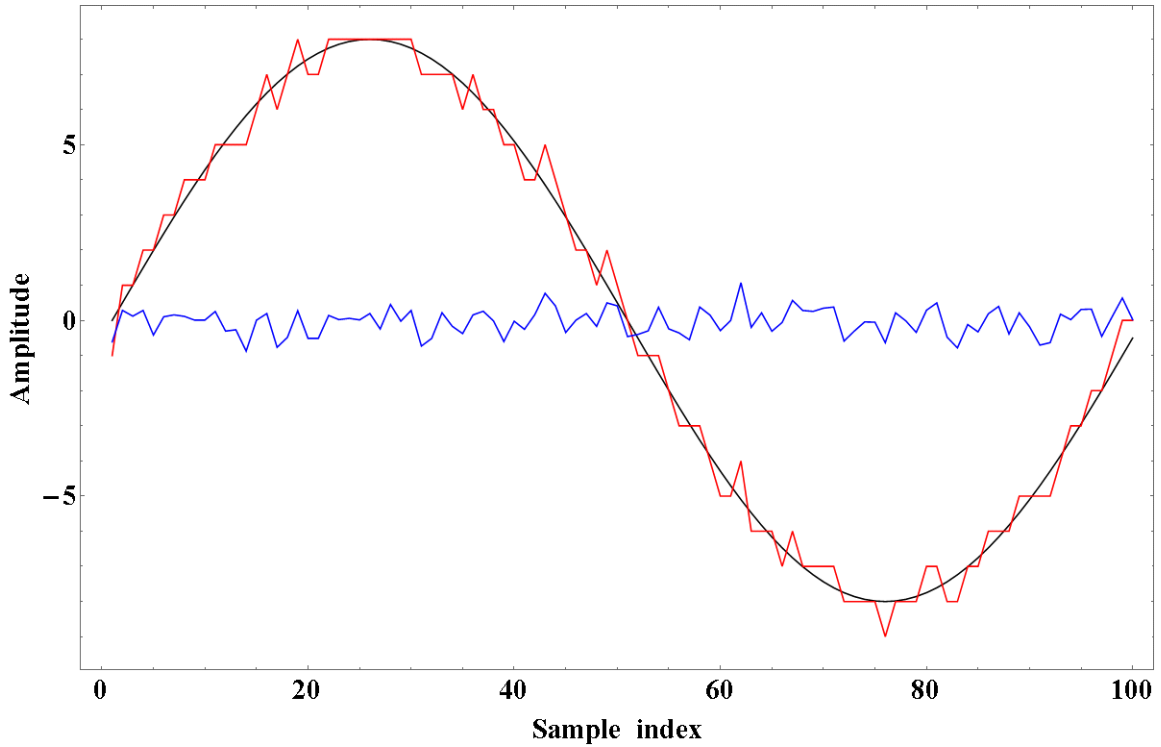


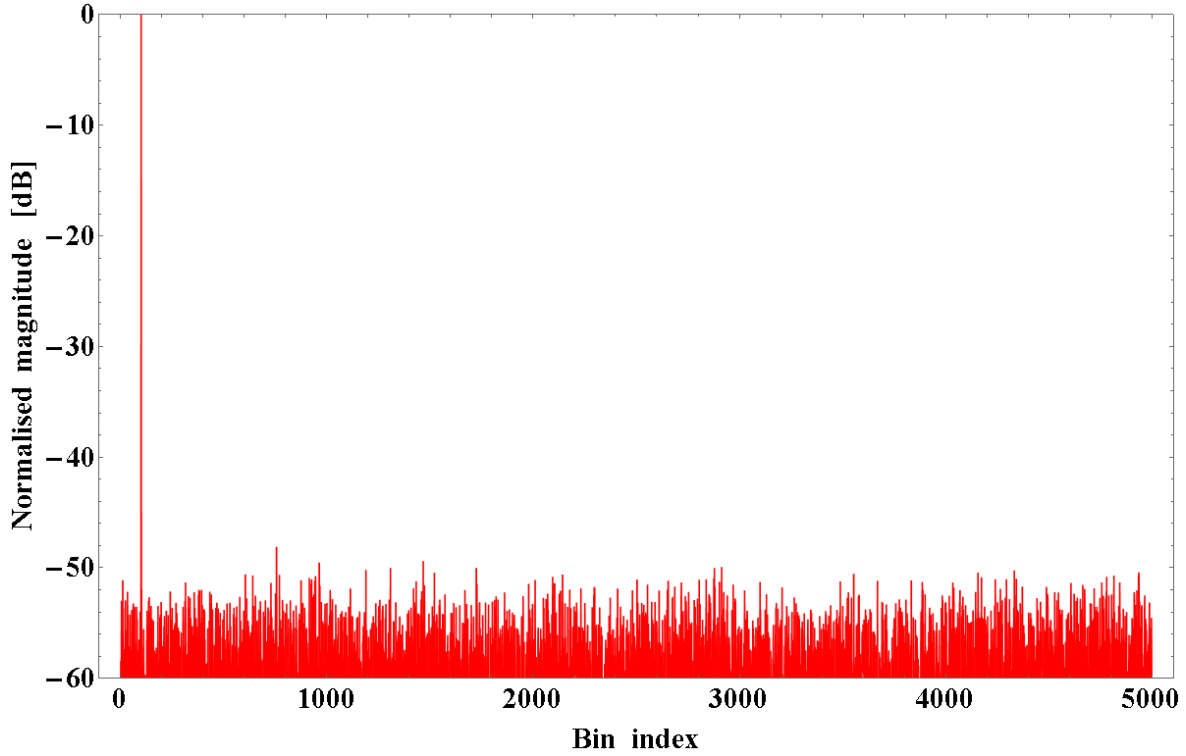


- N = 10000 samples of a full scale 4-bit sine
- f_{in} = 0.01 f_s (100 samples per s_{in} period)
- 100 samples of 1 period shown, corresponding to 1 % of the whole signal

- only one component expected, at $N \times f_{in} / f_s$, that is 100th bin
- Other components have levels in the order of – 40 dB, that is about 1 % of the fundamental

Quantization error and dither

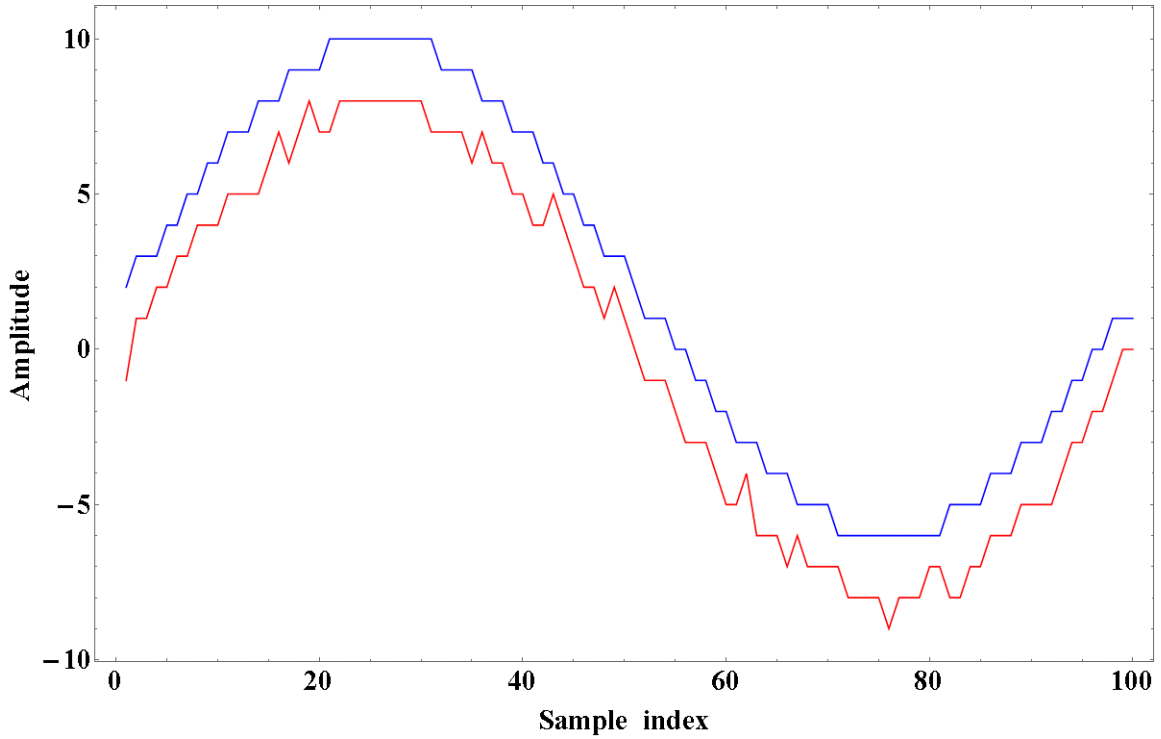


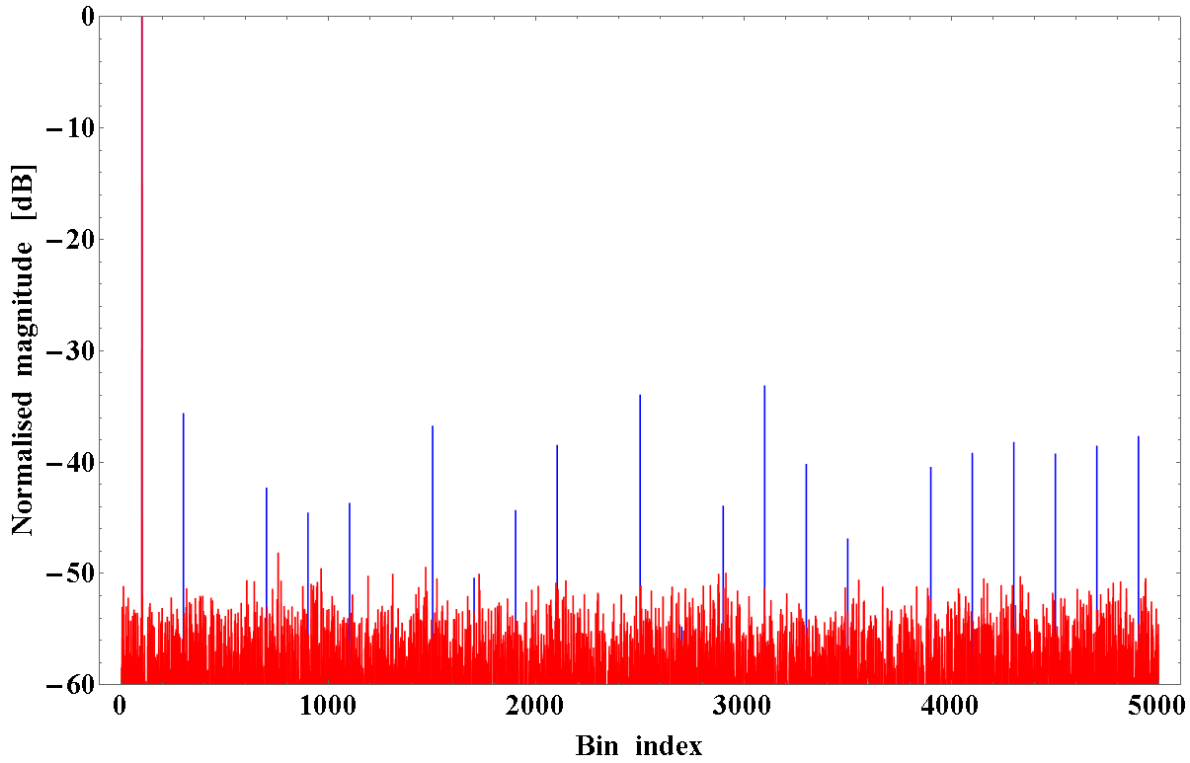


- As before, but added a small noise (blue) to the input signal, of RMS amplitude 0.4 *q*

- Now only one component seen at the expected location
- Noise floor seen at the level in the order of – 55 dB, that is about 0.18 % of the fundamental

No dither vs. dither

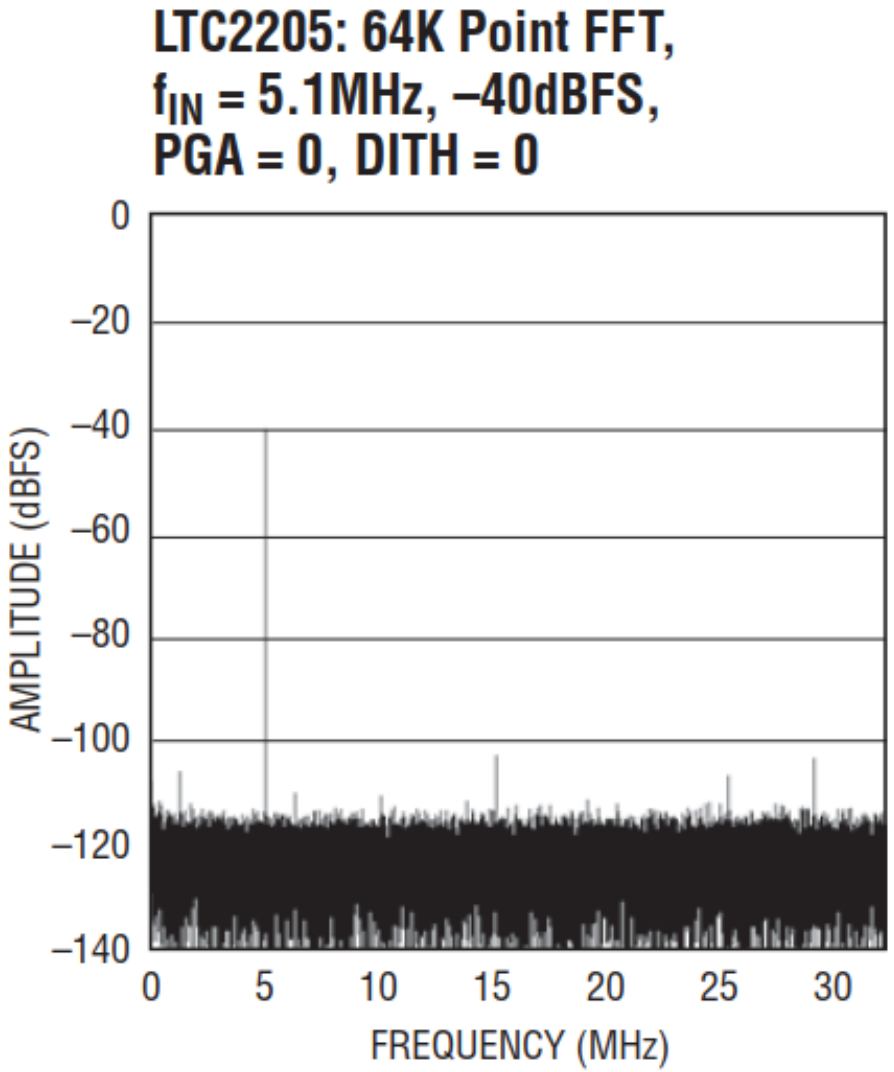


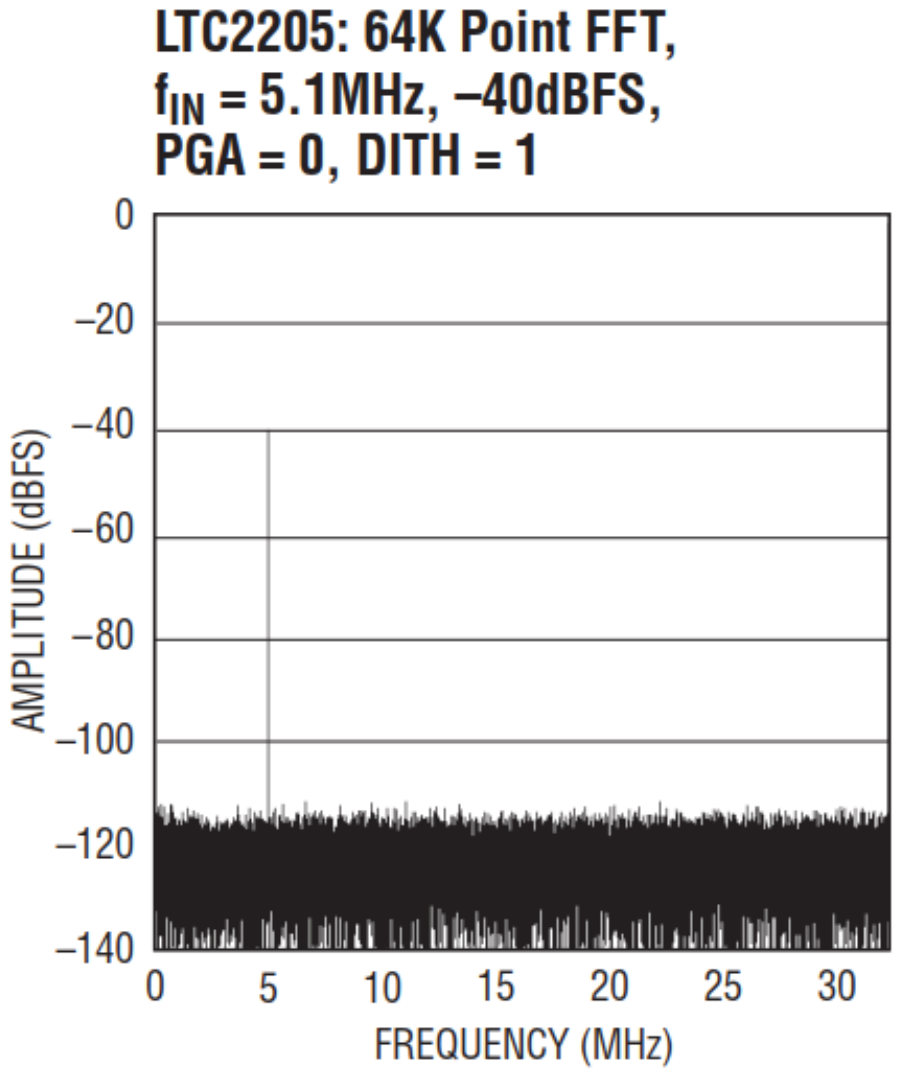


- In blue: input signal without noise (shifted vertically for better visibility)
- In red: input signal with noise

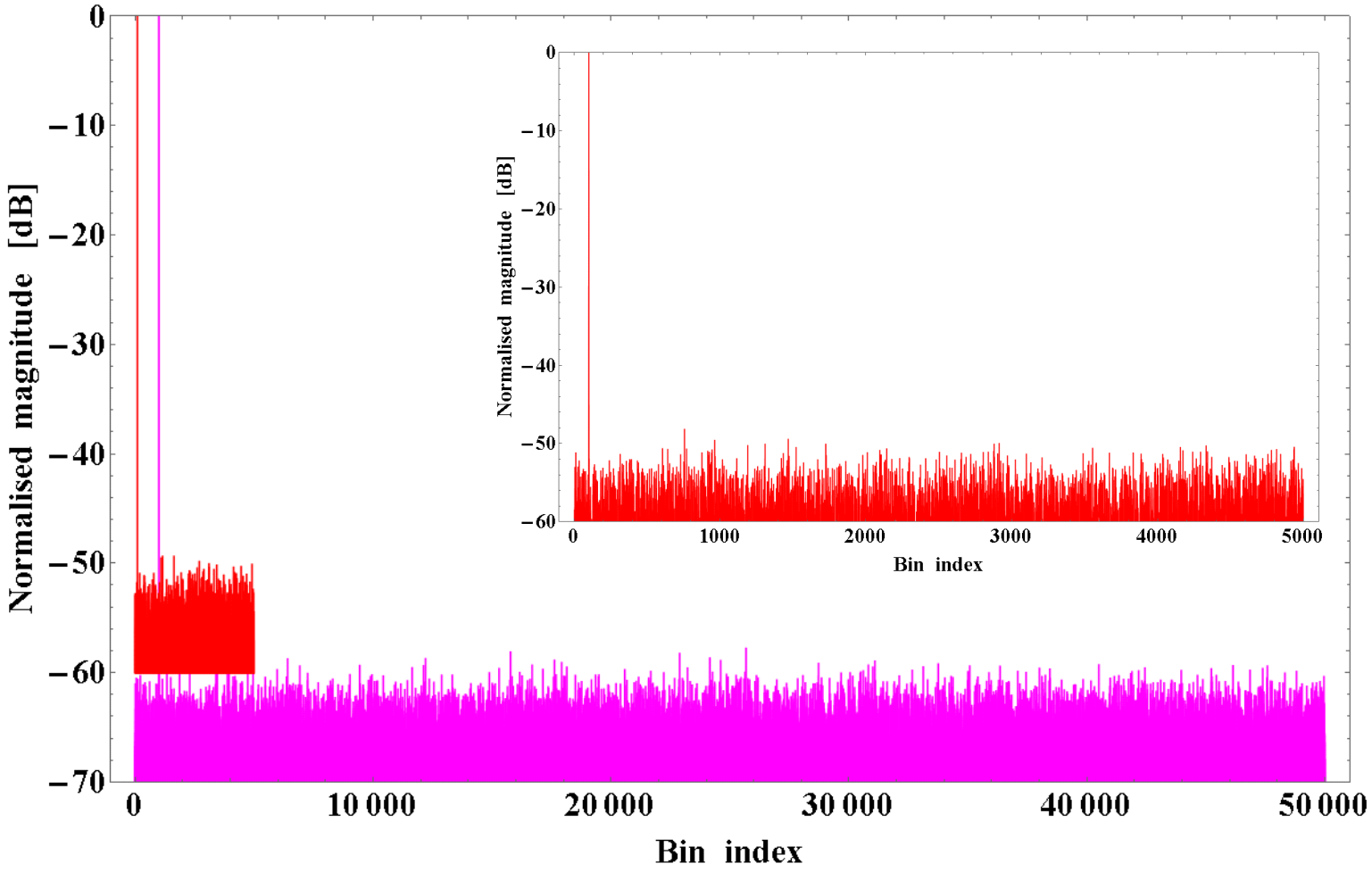
- In blue: spectrum of the signal without noise
- In red: spectrum of the signal with noise

To dither or not to dither





Discrete spectra: “FFT gain”

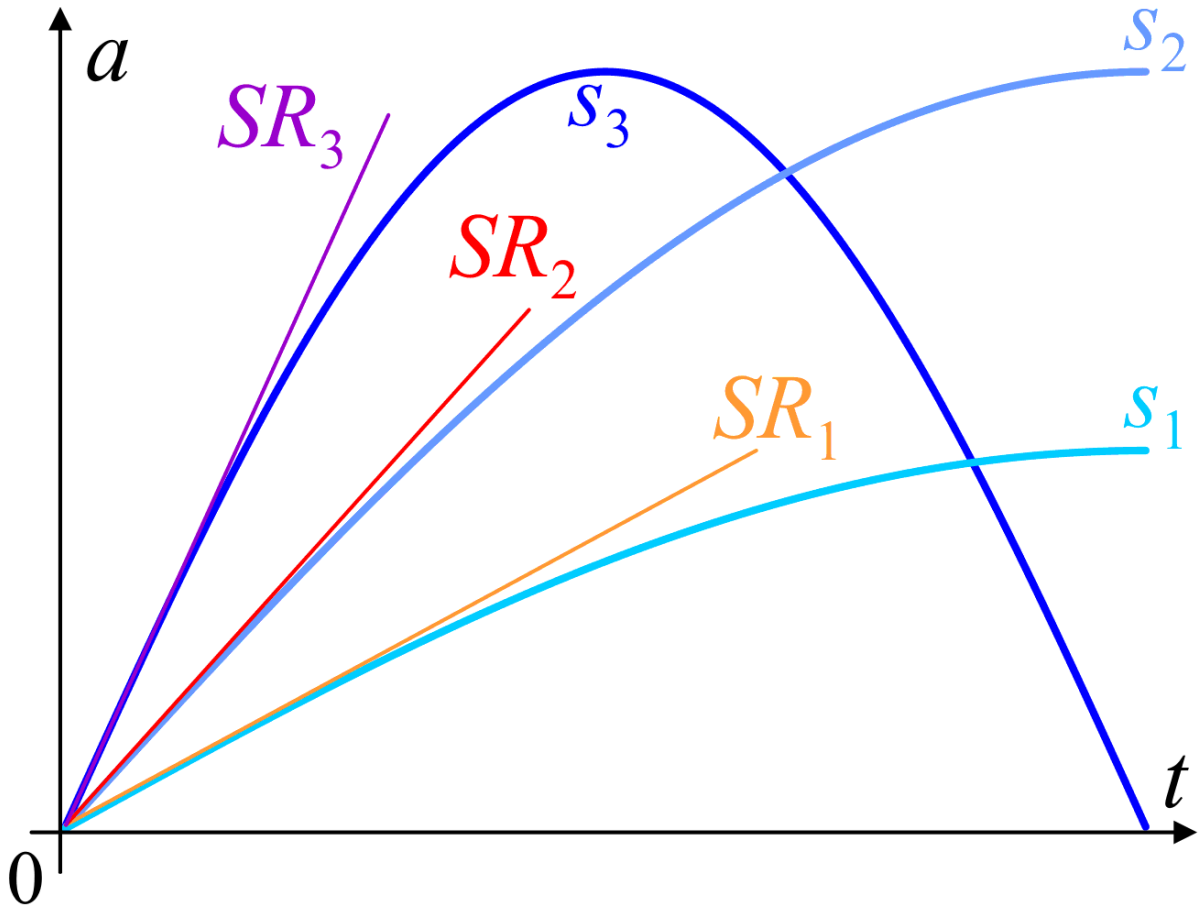


- In red: 10 kS spectrum as before
- In magenta: 100 kS spectrum
- N increased 10 times, noise decreased by 10 dB

- FFT gain = $\sqrt{\frac{1}{2}N}$

- FFT noise floor = $\frac{\text{time domain noise}}{\text{FFT gain}}$

Slew rate

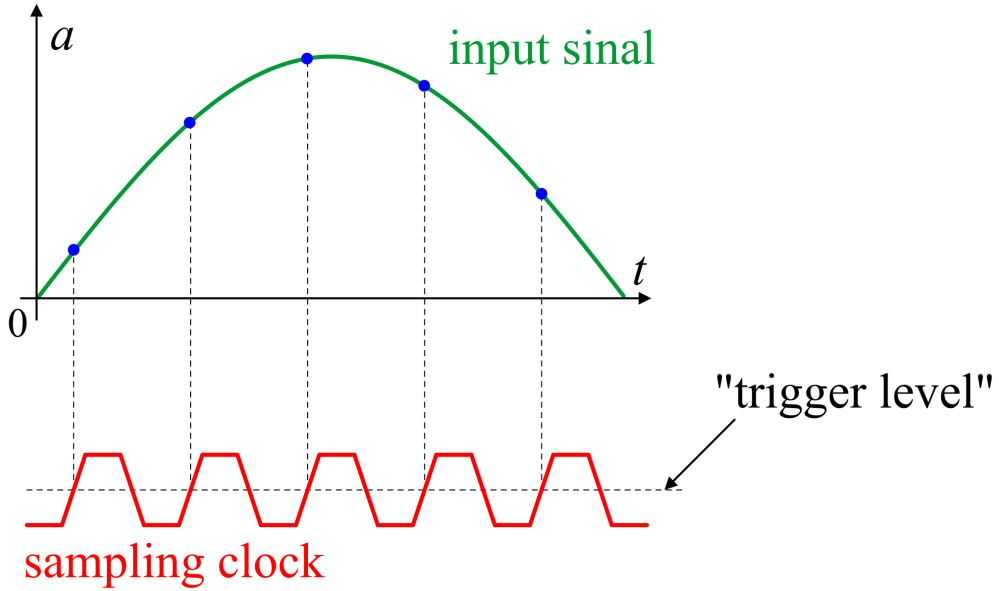


$$s(t) = A \sin 2\pi f t$$

$$SR = \max \frac{ds}{dt} = 2\pi A f$$

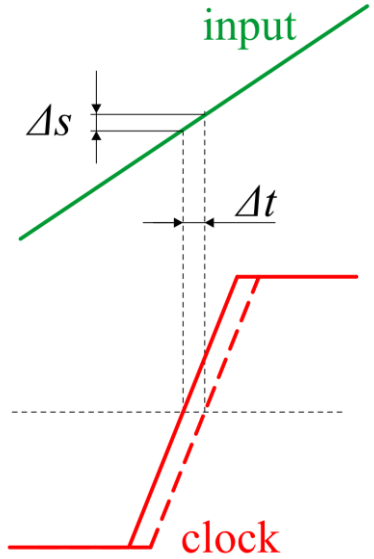
- Signals of higher frequency require better SR
- Larger signals require better SR
- Pulse signals faster than the circuit SR are distorted
- If SR hits the limit and still faster signals are required, then the only option is to limit the signal amplitude
- ADCs for GHz signals have small input dynamic range, sometimes below 1 Vpp
- Smaller amplitudes do not help for SNR

Clock jitter



- The sampling instances are defined by the clock signal
- Noise on the clock signal shifts the sampling instances, introducing amplitude errors of the sampled signal

$$\Delta s = \frac{ds}{dt}\Delta t$$



- Assuming a sine signal and that the amplitude noise due to the clock jitter is smaller than 0.5 LSB

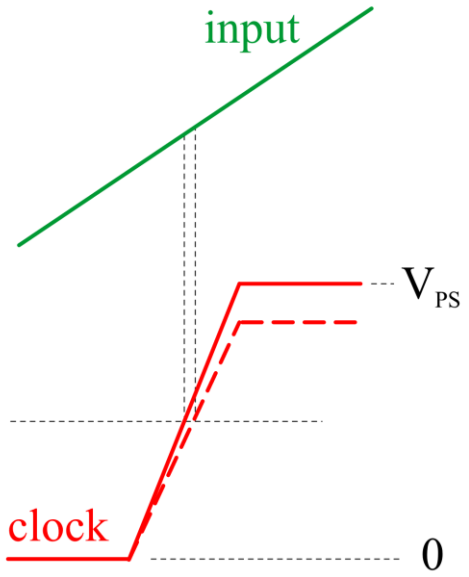
$$\Delta t < \frac{1}{2\pi f 2^n}$$

Clock jitter

$$\Delta t < \frac{1}{2\pi f 2^n}$$

Maximal clock jitter for erorrs < 0.5 LSB

f	8 bits	12 bits	16 bits	24 bits
1 kHz	620 ns	39 ns	2.4 ns	9.5 ps
1 MHz	620 ps	39 p	2.4 ps	9.5 fs
1 GHz	620 fs	39 fs	2.4 fs	9.5 as



- For faster ADCs with more bits a low jitter sampling clock is a challenge
- Fast ADCs have differential clock inputs
- Amplitude noise on the clock lines can also cause clock jitter, so very clean power supplies are required for the clock circuitry
- Clock signals should not be considered as digital signals but rather like super-sensitive analog signals
- Good clocks never come directly from an FPGA or other complex logic
- For high performance ADCs there are dedicated chips for producing clock signals with an adequate quality

Fundamental ADC limitations

- More bandwidth → more noise → smaller SNR

$$V_n = \sqrt{4kTRB}$$

- Faster signals → smaller amplitudes possible

$$f_{max} = \frac{\text{slew rate}}{2\pi A_{max}}$$

- Faster signals → larger switching currents required → larger power dissipation

$$\frac{du_c}{dt} = \frac{i_c}{C_p}$$

- Faster signals or more bits → smaller clock jitter required

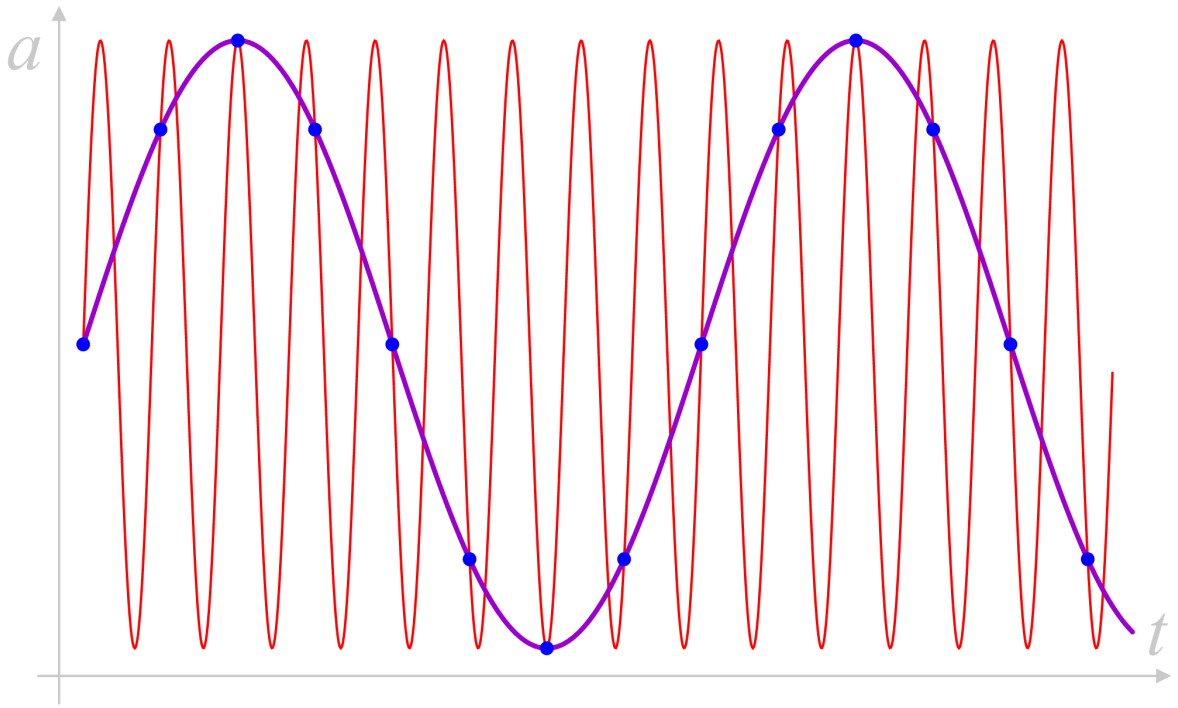
R = 50 Ω, T = 300 K

B	V_n	SNR_{5V}	SNR_{1V}	$ENOB_{5V}$	$ENOB_{1V}$
1 Hz	0.9 nV	186	172	30.6	28.2
1 kHz	29 nV	156	142	25.6	23.3
1 MHz	910 nV	126	112	20.6	18.3
1 GHz	29 µV	96	82	15.6	13.3

R = 1 kΩ, T = 300 K

B	V_n	SNR_{5V}	SNR_{1V}	$ENOB_{5V}$	$ENOB_{1V}$
1 Hz	4.1 nV	173	159	28.4	26.1
1 kHz	130 nV	143	129	23.4	21.1
1 MHz	4.1 µV	113	99	18.4	16.1
1 GHz	130 µV	83	69	13.5	11.1

Sampling



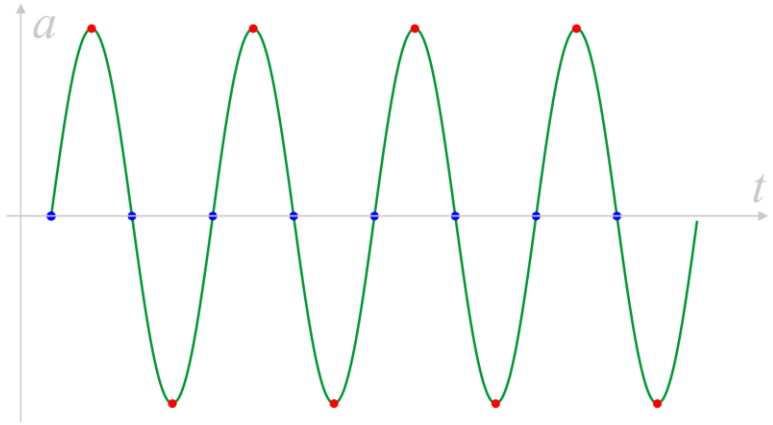
$$f_{sampling} > 2 \cdot (\text{signal bandwidth})$$

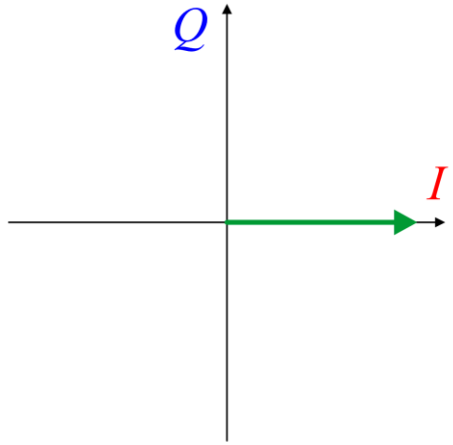
- The Niquist-Shannon sampling theorem:

  If a signal is sampled at least twice per period of the component with the highest frequency, then the signal
  can be perfectly reconstructed from the samples

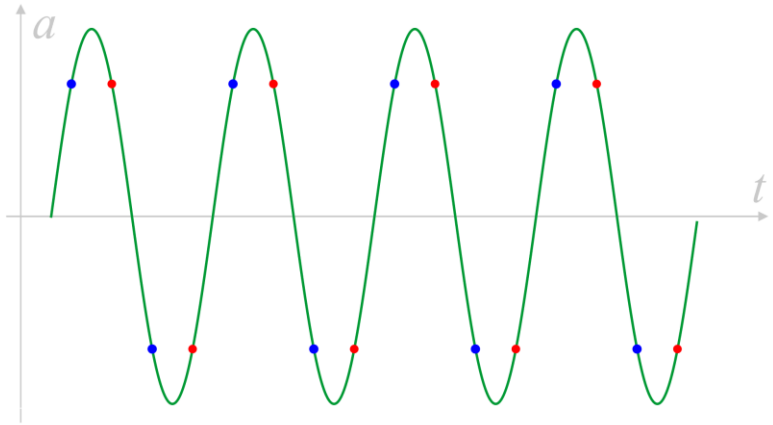
- Aliasing phenomenon, if the Niquist criterion is not respected
- Sometimes aliasing is a desired effect
- Aliasing cannot be compensated “in digital”
- The digitized signal must be band-limited (anti-aliasing filter)
- Because the filter needs some “frequency room” to develop the attenuation, the sampling rate should be higher than the theorem says
- The more oversampling, the easier the anti-aliasing filter

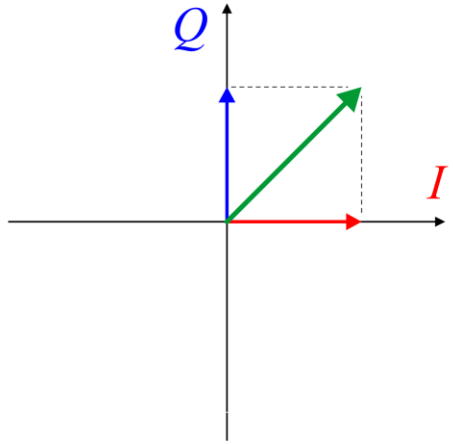
Sampling a sinewave: IQ demodulation





- “IQ demodulation” is a popular technique to digitize sine signals
- IQ demodulation needs the sampling clock to be synchronised to the input signal
- Exactly 4 samples per input signal period (2 × Niquist)
- I = “in phase”, Q = “quadrature”
- Amplitude and phase information





$$a = \sqrt{I^2 + Q^2}$$

$$\varphi = \arctan\frac{Q}{I}$$

Sampling a pulse

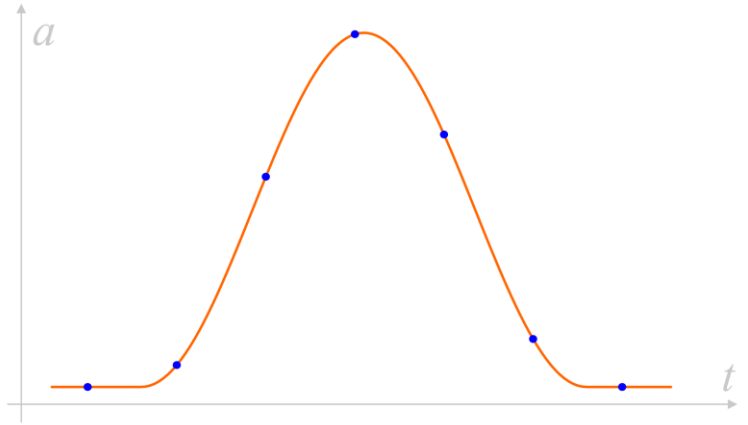
The ADC clock synchronised to $n \times f_{rev}$ or $n \times f_{RF}$

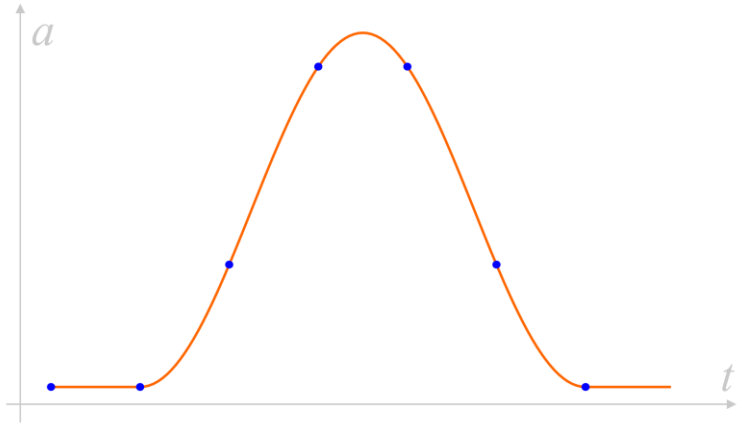
+ a few samples required to have good signal reconstruction
+ the sampling follows the machine frequency changes
– machine timing has to be delivered to the system
– machine timing necessary for proper operation
– often a local PLL necessary to get the required clock jitter
– phase adjustment w.r.t. the beam often required
– phase adjustment changes with the frequency

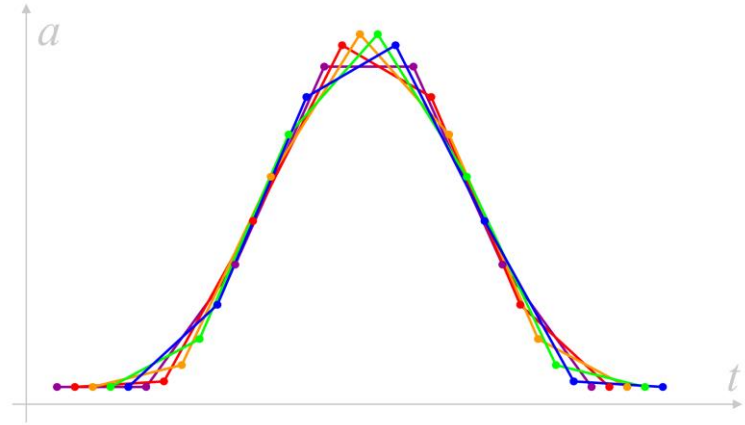
$$\Delta\varphi_{clk} = 2\pi\,\tau_{clk}\Delta f_{clk}$$

A fixed-frequency ADC clock generated locally

+ very simple and robust
+ best ADC clock quality possible
– random sampling phase
– more samples required for good signal reconstruction

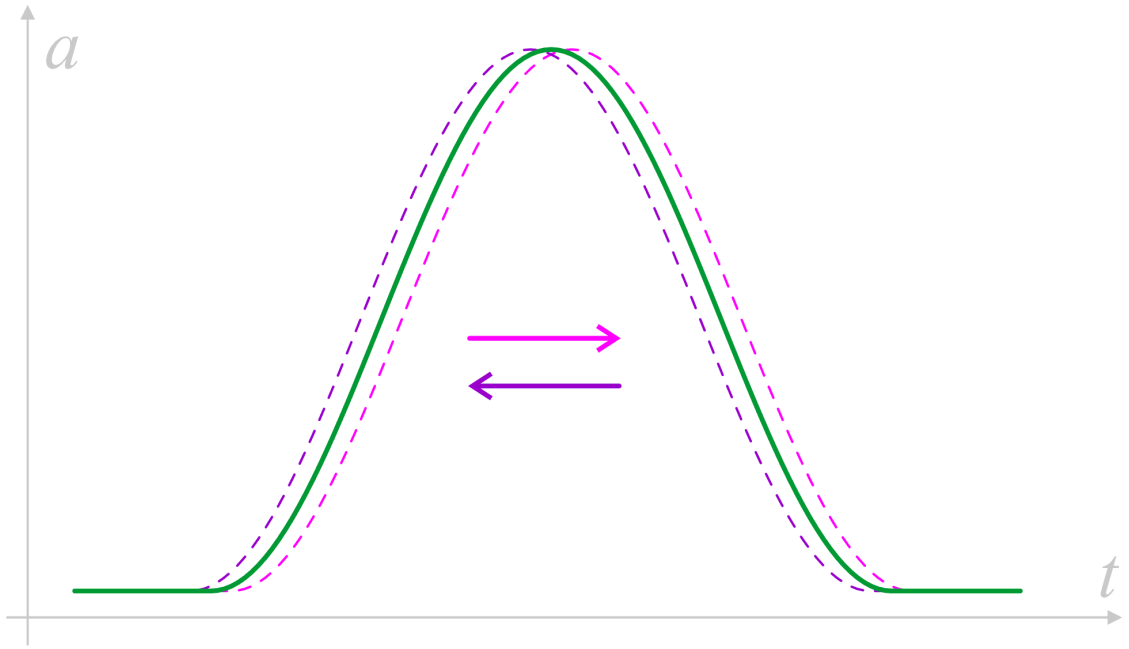


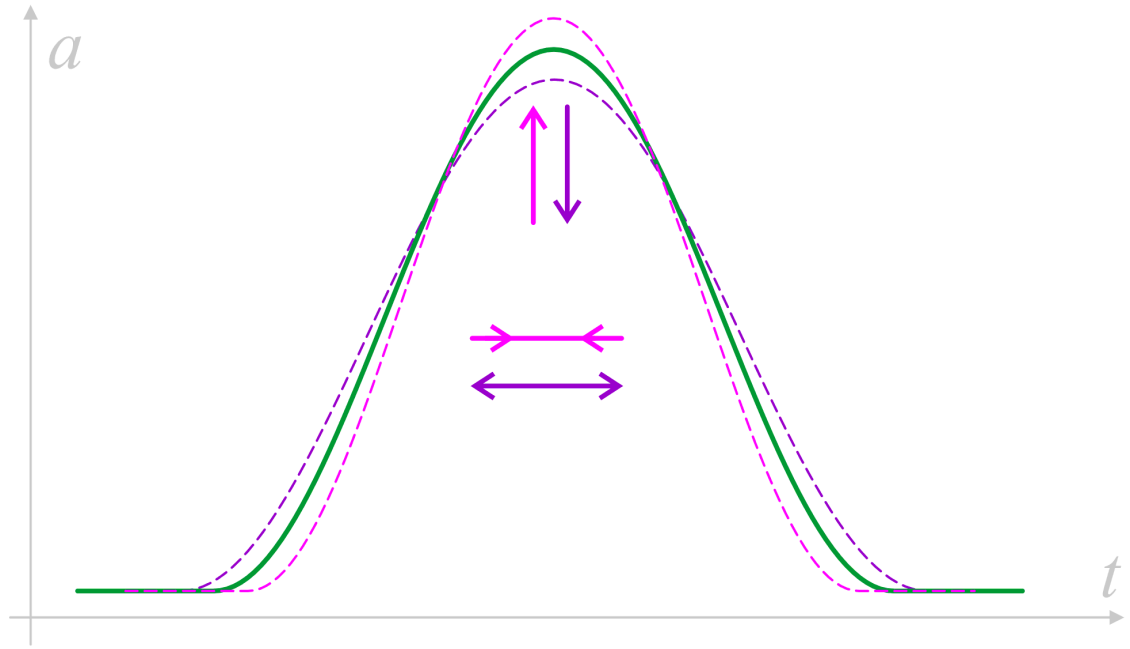




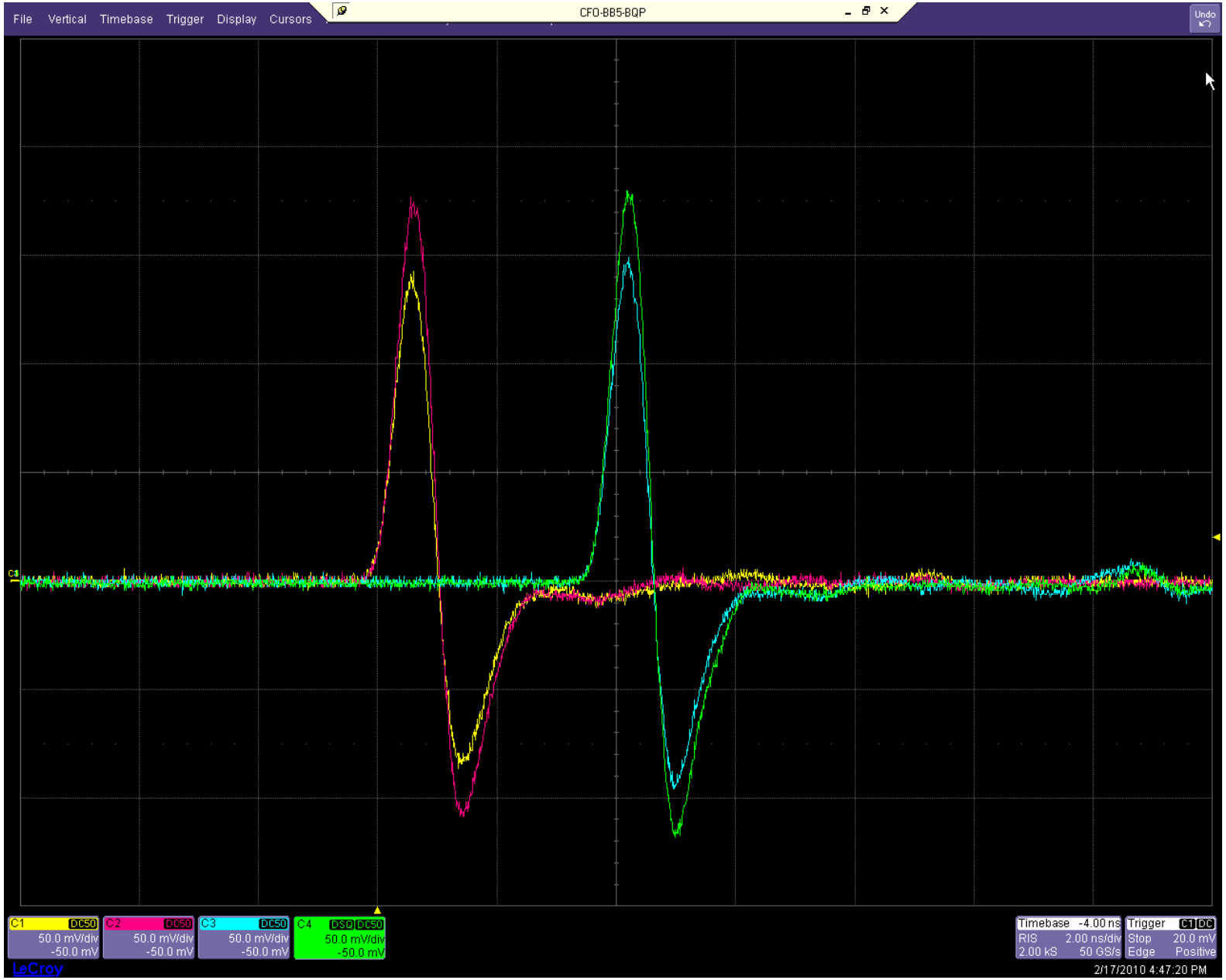
Sampling a pulse

- Beam signals are not static
- The beam signal phase changes due to synchrotron motion
- Beam signal shape follows the synchrotron motion
- Measuring the signals foreseen for digitisation is a good idea before choosing the sampling rate
- Adequate low pass filtering can reduce the phase and shape changes



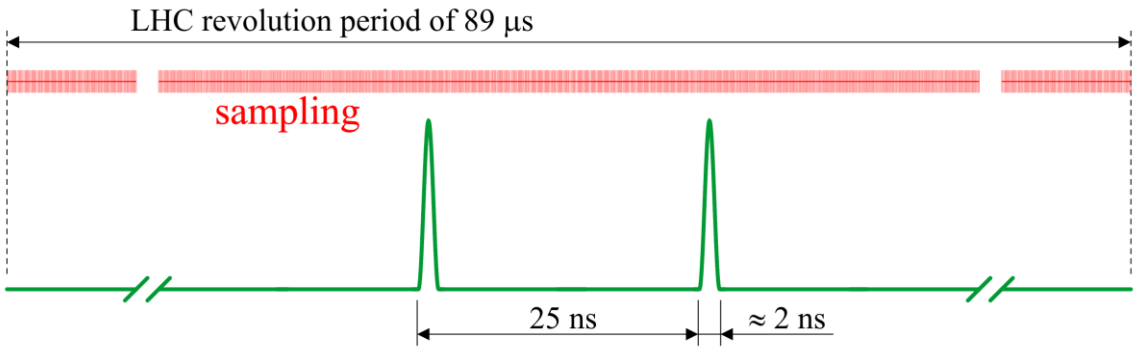


Sampling a pulse



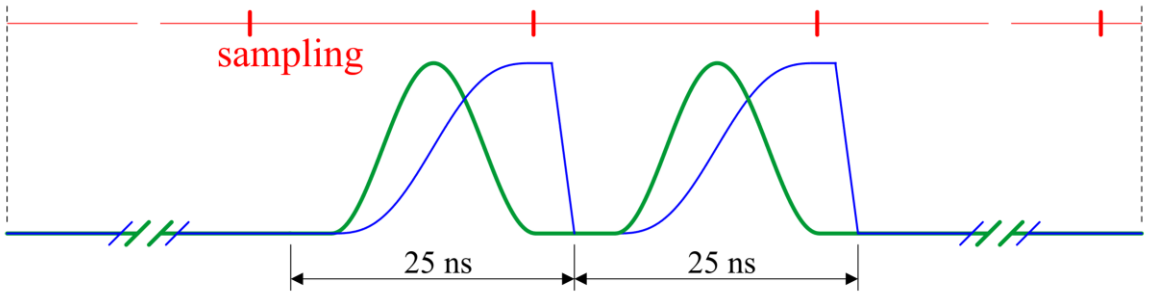
- 50 mV/div, 2 ns/div
- SPS beam
- 2 pairs of 10 mm button electrodes
- Signals already “filtered” by quite long cables

What sampling rate do I need ?



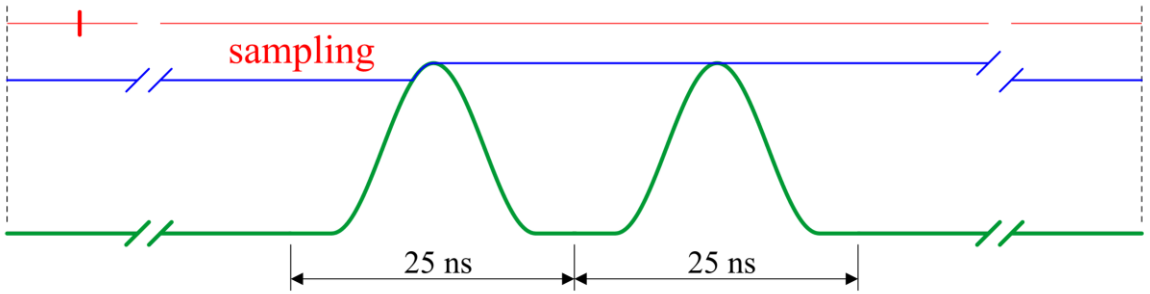
Beam position within a bunch (“head-tail” system)

- BPM signal direct sampling with a fast oscilloscope
- analogue BW 4 GHz, 10 GS/s, 10 bits, ENOB 8.7
- 890 kS/turn, 12.5 GB/s



Beam position per bunch (“normaliser” system, “S-normaliser”)

- bunch position → time interval → voltage → number
- analogue BW 70 MHz, 40 MS/s, 10 (16) bits, ENOB 9.5 (12.8)
- 3.6 kS/turn, 50 (80) MB/s



Beam position per turn (“diode” system)

- peak bunch amplitude → DC voltage → number
- analogue BW 100 Hz, 11 kS/s, 24 bits, ENOB 18.0
- 1 S/turn, 34 kB/s

What sampling rate do I need ?

- The “good” sampling rate depends on
  - the time structure of the digitized signal
  - the required time resolution of the measured quantity: specification needed !
  - the analog processing possible before the ADC
  - the size of the system and the available money and manpower

- Faster sampling is expensive:
  - poorer resolution
  - often smaller input dynamic range
  - more samples to take care of
  - higher power dissipation
  - the ADC itself costs more
  - the FPGA receiving the ADC data costs more
  - more complex system and data processing (more work required)

How many bits do I need ?

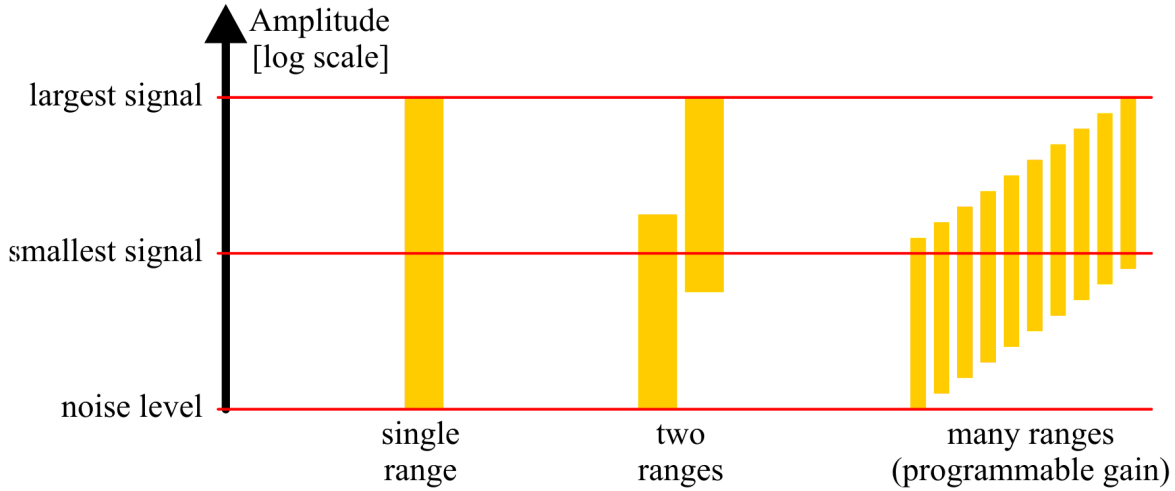
Example on LHC beam intensity measurements (DCCT): DC beam current integral

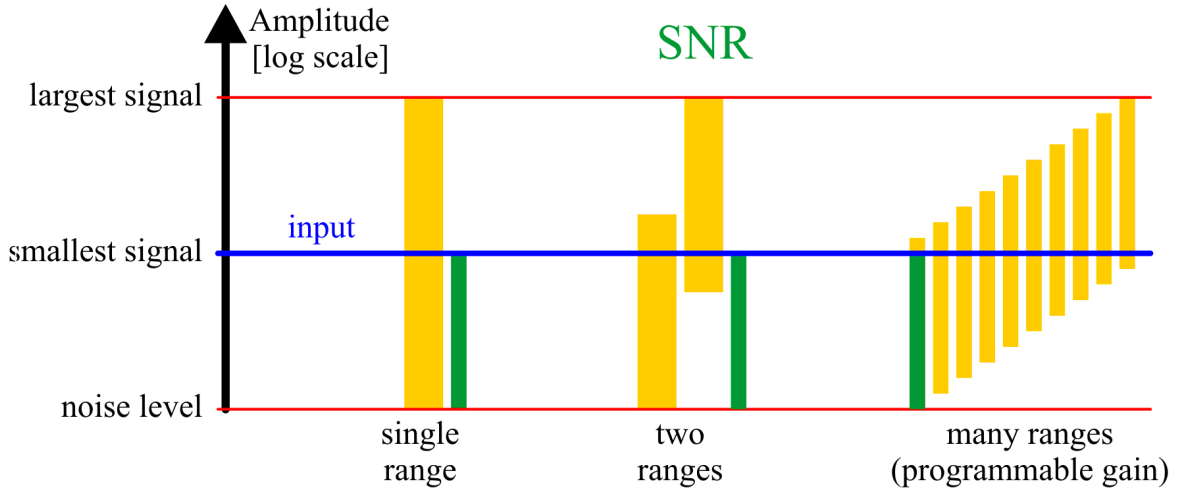
- Single pilot bunch 5×10^9: required resolution 1% (well below noise of the sensor + electronics)
- Nominal bunch + margin: 3×10^{11} (pilot × 60)
- Max. number of bunches 3000

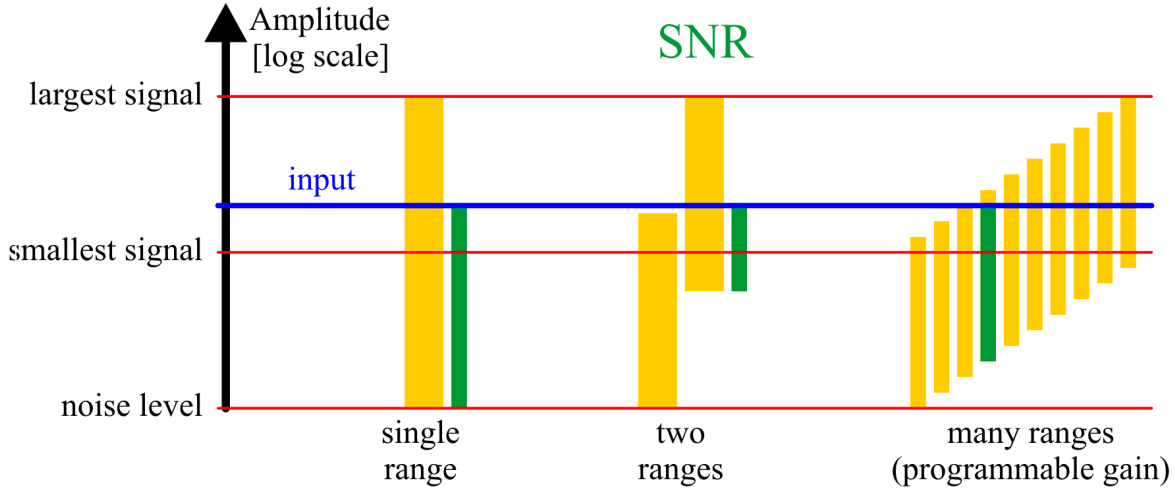
- Required dynamic range: $100 \times 60 \times 3000 = 18 \times 10^6$
- Required number of bits: $\log_2(18 \times 10^6) = 24.1$

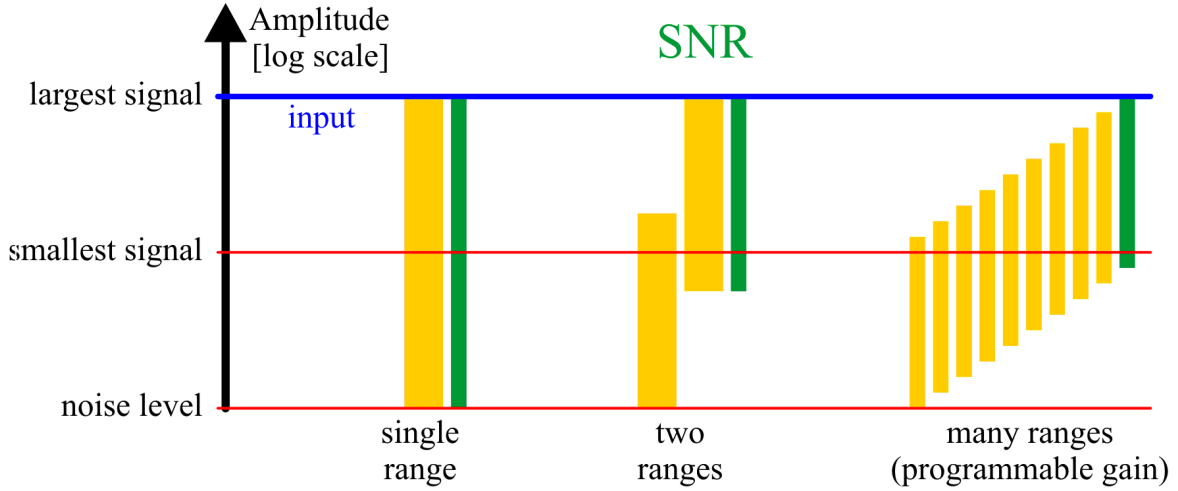
- Signal is slow, so a 24-bit ADC possible (and used in reality)
- A good 24-bit ADC has some 110 dB SNR, that is some 18 bits
- 6 bits missing, a factor of 64
- Room for SNR improvement by averaging: required averaging factor $64^2 = 4096$
  If the acquisition is done once per turn, then the 4096 average lasts $4096/11246 \approx 0.4$ s
- Averaging could be replaced by an IIR filtering

How many bits do I need ?

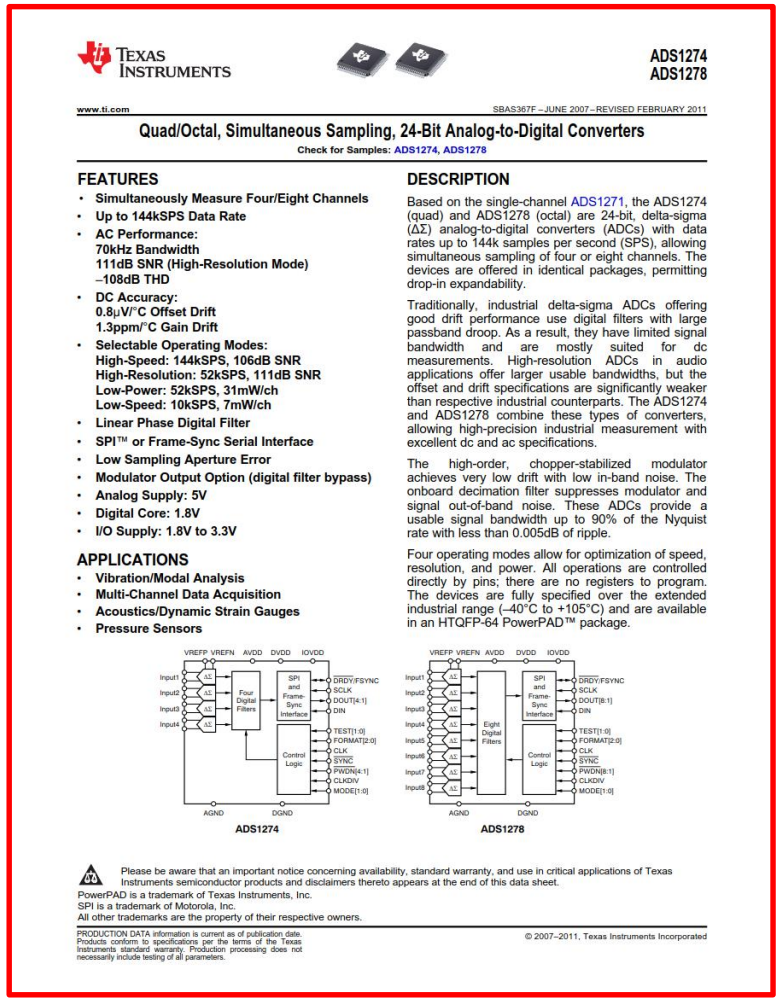








Comparison



TEXAS INSTRUMENTS

ADS1274
ADS1278

www.ti.com — SBAS367F – JUNE 2007 – REVISED FEBRUARY 2011

Quad/Octal, Simultaneous Sampling, 24-Bit Analog-to-Digital Converters

Check for Samples: ADS1274, ADS1278

FEATURES

- Simultaneously Measure Four/Eight Channels
- Up to 144kSPS Data Rate
- AC Performance:
  70kHz Bandwidth
  111dB SNR (High-Resolution Mode)
  –108dB THD
- DC Accuracy:
  0.8μV/°C Offset Drift
  1.3ppm/°C Gain Drift
- Selectable Operating Modes:
  High-Speed: 144kSPS, 106dB SNR
  High-Resolution: 52kSPS, 111dB SNR
  Low-Power: 52kSPS, 31mW/ch
  Low-Speed: 10kSPS, 7mW/ch
- Linear Phase Digital Filter
- SPI™ or Frame-Sync Serial Interface
- Low Sampling Aperture Error
- Modulator Output Option (digital filter bypass)
- Analog Supply: 5V
- Digital Core: 1.8V
- I/O Supply: 1.8V to 3.3V

APPLICATIONS

- Vibration/Modal Analysis
- Multi-Channel Data Acquisition
- Acoustics/Dynamic Strain Gauges
- Pressure Sensors

DESCRIPTION

Based on the single-channel ADS1271, the ADS1274 (quad) and ADS1278 (octal) are 24-bit, delta-sigma (ΔΣ) analog-to-digital converters (ADCs) with data rates up to 144k samples per second (SPS), allowing simultaneous sampling of four or eight channels. The devices are offered in identical packages, permitting drop-in expandability.

Traditionally, industrial delta-sigma ADCs offering good drift performance use digital filters with large passband droop. As a result, they have limited signal bandwidth and are mostly suited for dc measurements. High-resolution ADCs in audio applications offer larger usable bandwidths, but the offset and drift specifications are significantly weaker than respective industrial counterparts. The ADS1274 and ADS1278 combine these types of converters, allowing high-precision industrial measurement with excellent dc and ac specifications.

The high-order, chopper-stabilized modulator achieves very low drift with low in-band noise. The onboard decimation filter suppresses modulator and signal out-of-band noise. These ADCs provide a usable signal bandwidth up to 90% of the Nyquist rate with less than 0.005dB of ripple.

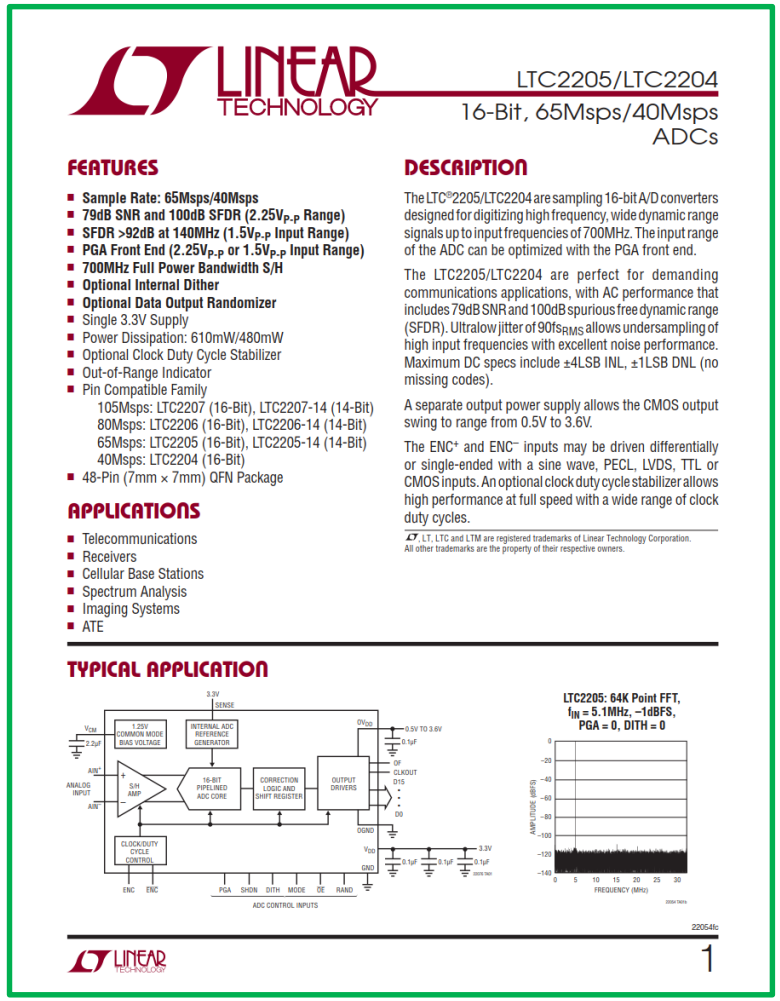
Four operating modes allow for optimization of speed, resolution, and power. All operations are controlled directly by pins; there are no registers to program. The devices are fully specified over the extended industrial range (–40°C to +105°C) and are available in an HTQFP-64 PowerPAD™ package.

ADS1274 ADS1278

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments, Inc.
SPI is a trademark of Motorola, Inc.
All other trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



LINEAR TECHNOLOGY

LTC2205/LTC2204
16-Bit, 65Msps/40Msps ADCs

FEATURES

- Sample Rate: 65Msps/40Msps
- 79dB SNR and 100dB SFDR (2.25V$_{P-P}$ Range)
- SFDR >92dB at 140MHz (1.5V$_{P-P}$ Input Range)
- PGA Front End (2.25V$_{P-P}$ or 1.5V$_{P-P}$ Input Range)
- 700MHz Full Power Bandwidth S/H
- Optional Internal Dither
- Optional Data Output Randomizer
- Single 3.3V Supply
- Power Dissipation: 610mW/480mW
- Optional Clock Duty Cycle Stabilizer
- Out-of-Range Indicator
- Pin Compatible Family
  105Msps: LTC2207 (16-Bit), LTC2207-14 (14-Bit)
  80Msps: LTC2206 (16-Bit), LTC2206-14 (14-Bit)
  65Msps: LTC2205 (16-Bit), LTC2205-14 (14-Bit)
  40Msps: LTC2204 (16-Bit)
- 48-Pin (7mm × 7mm) QFN Package

APPLICATIONS

- Telecommunications
- Receivers
- Cellular Base Stations
- Spectrum Analysis
- Imaging Systems
- ATE

DESCRIPTION

The LTC®2205/LTC2204 are sampling 16-bit A/D converters designed for digitizing high frequency, wide dynamic range signals up to input frequencies of 700MHz. The input range of the ADC can be optimized with the PGA front end.

The LTC2205/LTC2204 are perfect for demanding communications applications, with AC performance that includes 79dB SNR and 100dB spurious free dynamic range (SFDR). Ultralow jitter of 90fs$_{RMS}$ allows undersampling of high input frequencies with excellent noise performance. Maximum DC specs include ±4LSB INL, ±1LSB DNL (no missing codes).

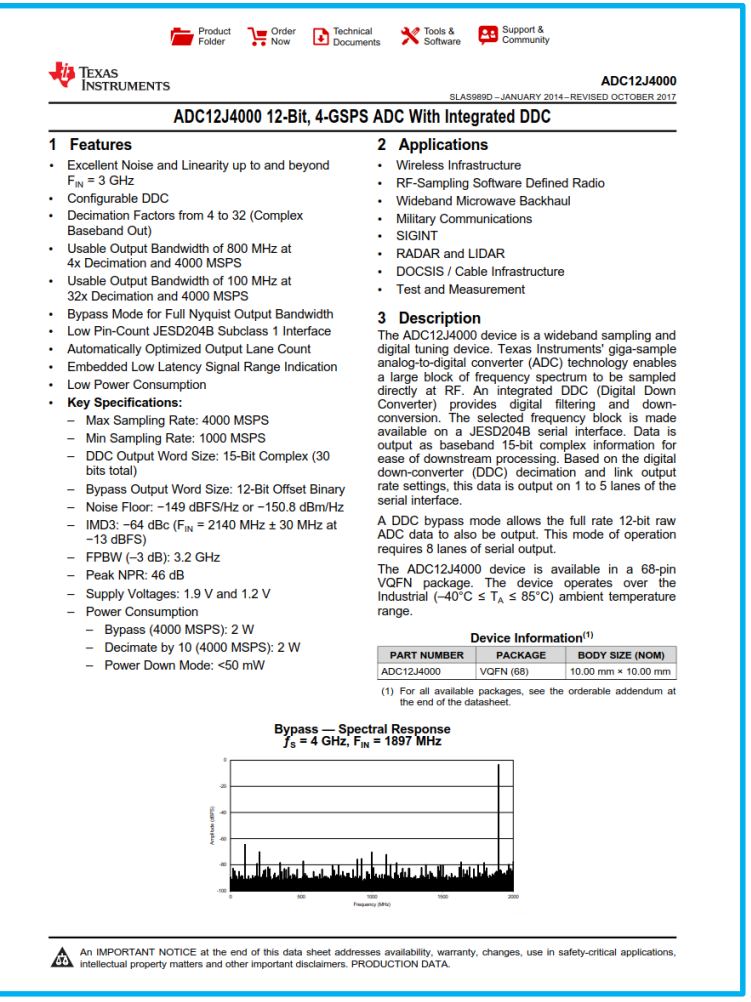
A separate output power supply allows the CMOS output swing to range from 0.5V to 3.6V.

The ENC$^+$ and ENC$^-$ inputs may be driven differentially or single-ended with a sine wave, PECL, LVDS, TTL or CMOS inputs. An optional clock duty cycle stabilizer allows high performance at full speed with a wide range of clock duty cycles.

TYPICAL APPLICATION

LTC2205: 64K Point FFT, f_{IN} = 5.1MHz, –1dBFS, PGA = 0, DITH = 0

220541c



Product Folder | Order Now | Technical Documents | Tools & Software | Support & Community

TEXAS INSTRUMENTS

ADC12J4000
SLAS989D – JANUARY 2014 – REVISED OCTOBER 2017

ADC12J4000 12-Bit, 4-GSPS ADC With Integrated DDC

1 Features

- Excellent Noise and Linearity up to and beyond F_{IN} = 3 GHz
- Configurable DDC
- Decimation Factors from 4 to 32 (Complex Baseband Out)
- Usable Output Bandwidth of 800 MHz at 4x Decimation and 4000 MSPS
- Usable Output Bandwidth of 100 MHz at 32x Decimation and 4000 MSPS
- Bypass Mode for Full Nyquist Output Bandwidth
- Low Pin-Count JESD204B Subclass 1 Interface
- Automatically Optimized Output Lane Count
- Embedded Low Latency Signal Range Indication
- Low Power Consumption
- **Key Specifications:**
  - Max Sampling Rate: 4000 MSPS
  - Min Sampling Rate: 1000 MSPS
  - DDC Output Word Size: 15-Bit Complex (30 bits total)
  - Bypass Output Word Size: 12-Bit Offset Binary
  - Noise Floor: −149 dBFS/Hz or −150.8 dBm/Hz
  - IMD3: −64 dBc (F_{IN} = 2140 MHz ± 30 MHz at −13 dBFS)
  - FPBW (–3 dB): 3.2 GHz
  - Peak NPR: 46 dB
  - Supply Voltages: 1.9 V and 1.2 V
  - Power Consumption
    - Bypass (4000 MSPS): 2 W
    - Decimate by 10 (4000 MSPS): 2 W
    - Power Down Mode: <50 mW

2 Applications

- Wireless Infrastructure
- RF-Sampling Software Defined Radio
- Wideband Microwave Backhaul
- Military Communications
- SIGINT
- RADAR and LIDAR
- DOCSIS / Cable Infrastructure
- Test and Measurement

3 Description

The ADC12J4000 device is a wideband sampling and digital tuning device. Texas Instruments' giga-sample analog-to-digital converter (ADC) technology enables a large block of frequency spectrum to be sampled directly at RF. An integrated DDC (Digital Down Converter) provides digital filtering and down-conversion. The selected frequency block is made available on a JESD204B serial interface. Data is output as baseband 15-bit complex information for ease of downstream processing. Based on the digital down-converter (DDC) decimation and link output rate settings, this data is output on 1 to 5 lanes of the serial interface.

A DDC bypass mode allows the full rate 12-bit raw ADC data to also be output. This mode of operation requires 8 lanes of serial output.

The ADC12J4000 device is available in a 68-pin VQFN package. The device operates over the Industrial (–40°C ≤ T_A ≤ 85°C) ambient temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADC12J4000	VQFN (68)	10.00 mm × 10.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Bypass — Spectral Response
f_S = 4 GHz, F_{IN} = 1897 MHz

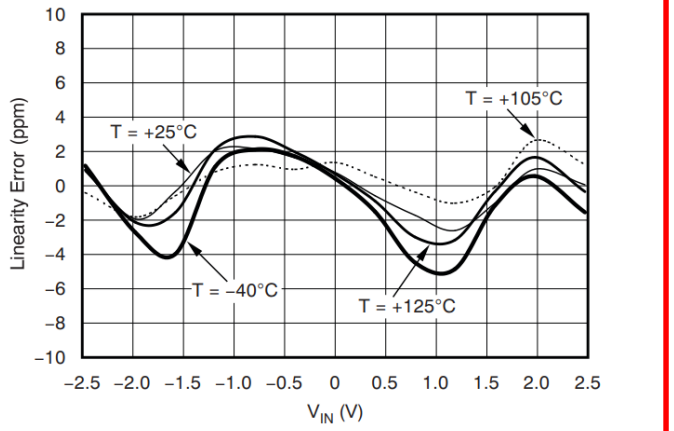
An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

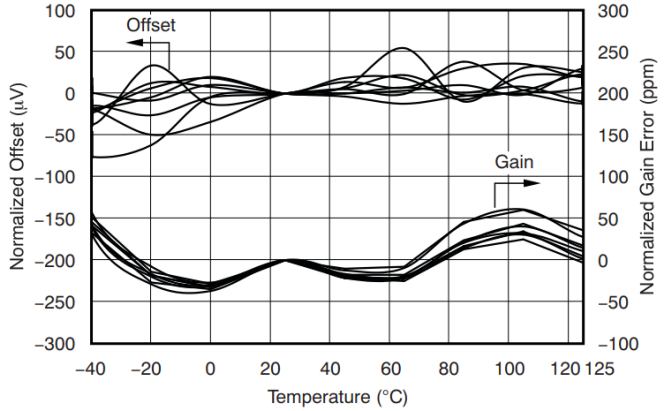
- 24 bits, ENOB 18.0, 144 kS/s, BW 78 kHz
- FS: 5 V, LSB: 0.3 μV
- 8 channels sampled in parallel

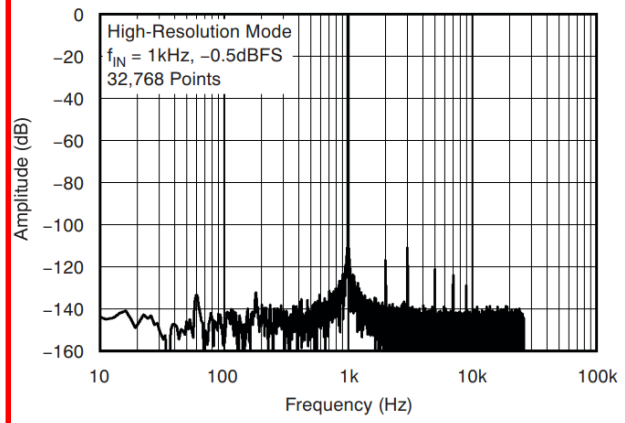
- 16 bits, ENOB 12.8, 65 MS/s, BW 700 MHz
- FS: 2.25 V, LSB: 34 μV
- A member of a large pin compatible family

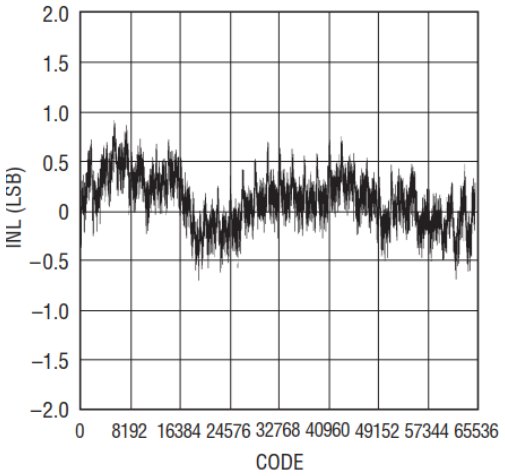
- 12 bits, ENOB 8.0, 4 GS/s, BW 3 GHz
- FS: 0.95 V, LSB: 230 μV
- Power consumption 2 W

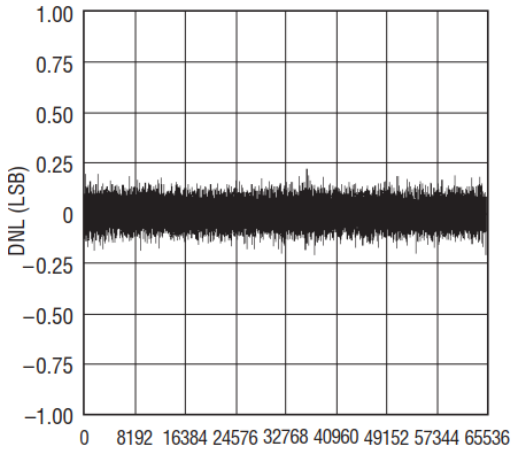
Comparison

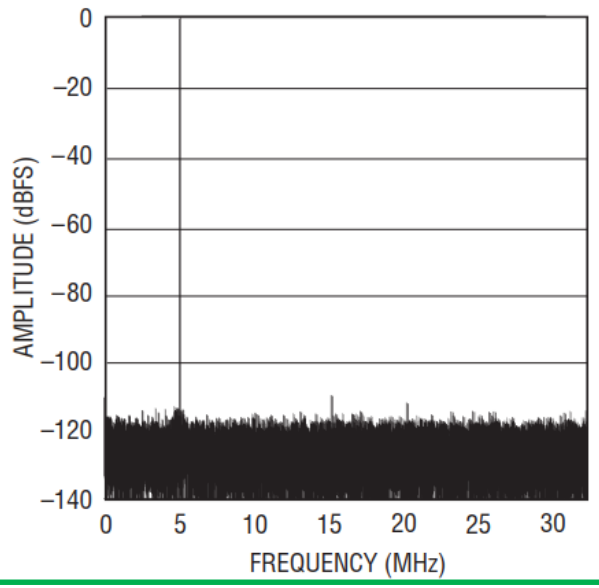


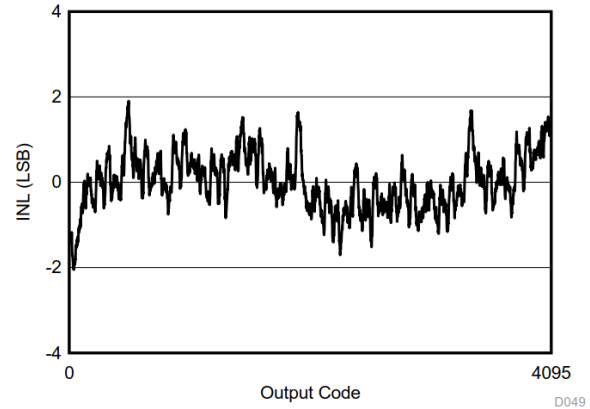


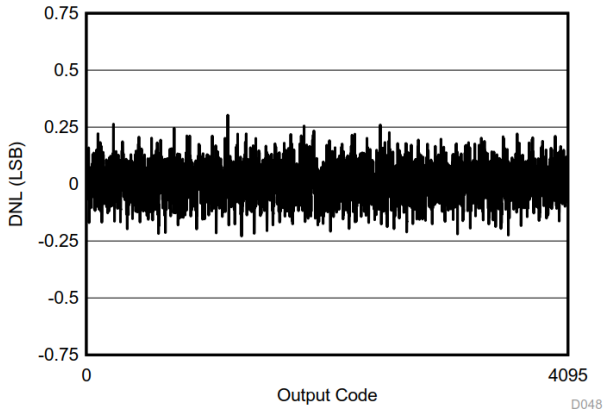


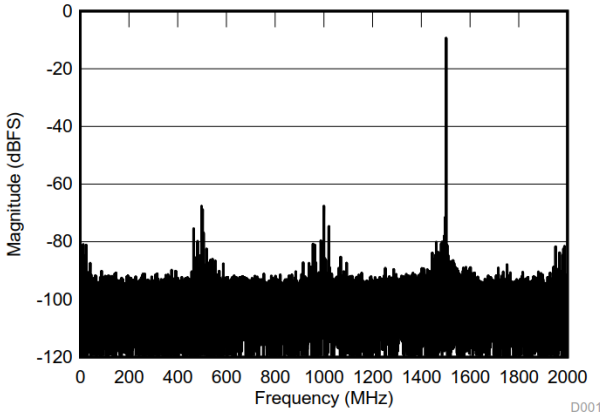






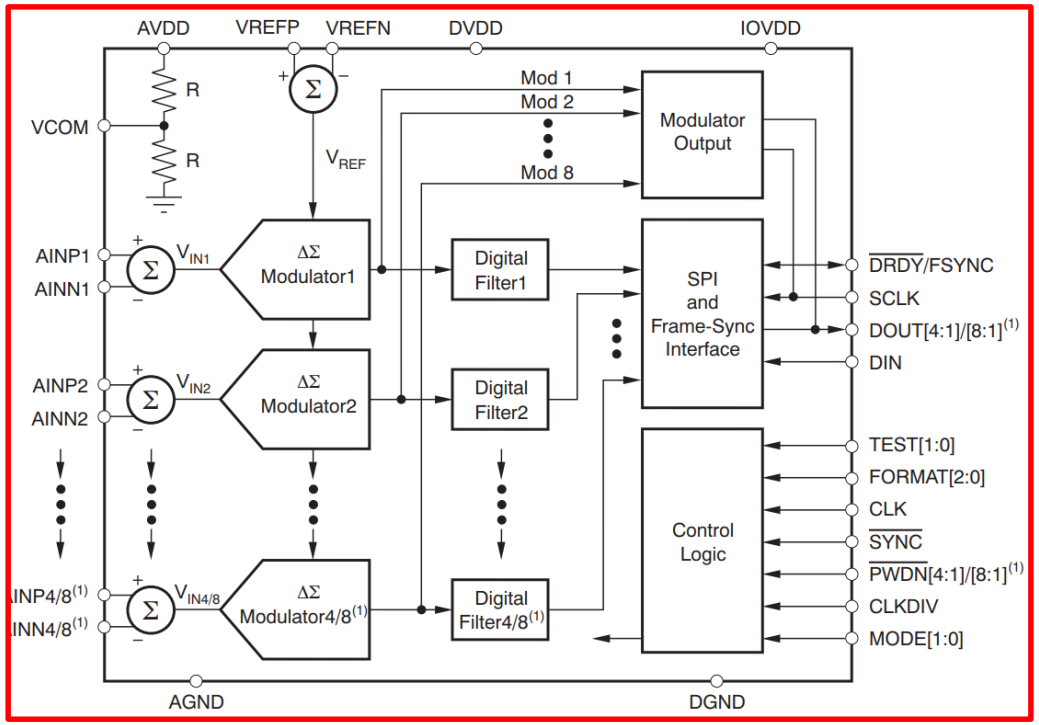


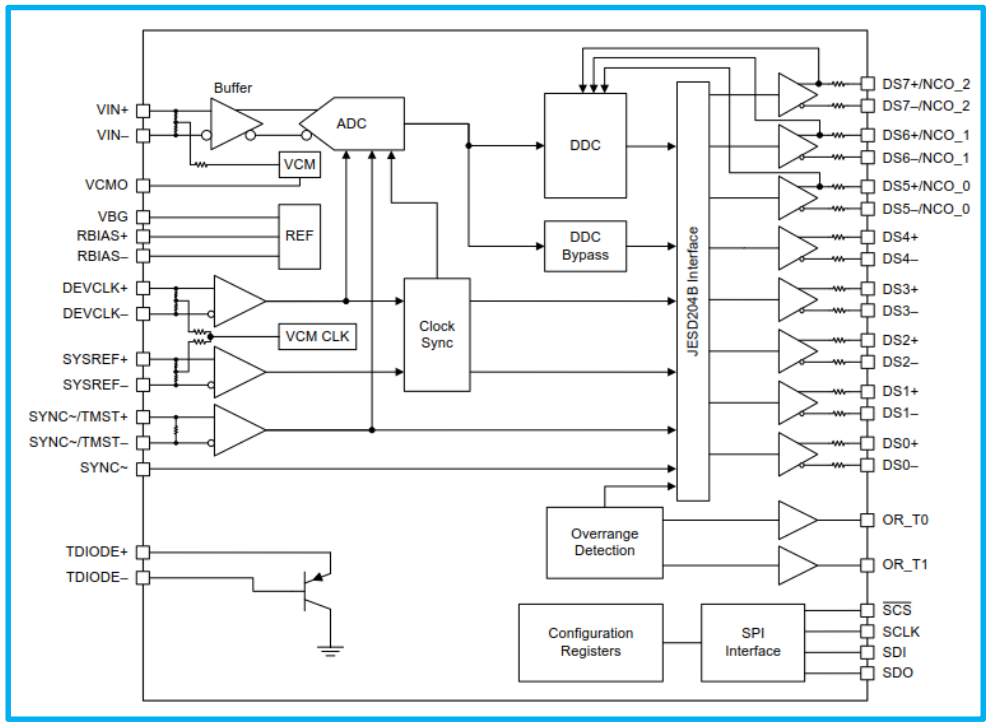


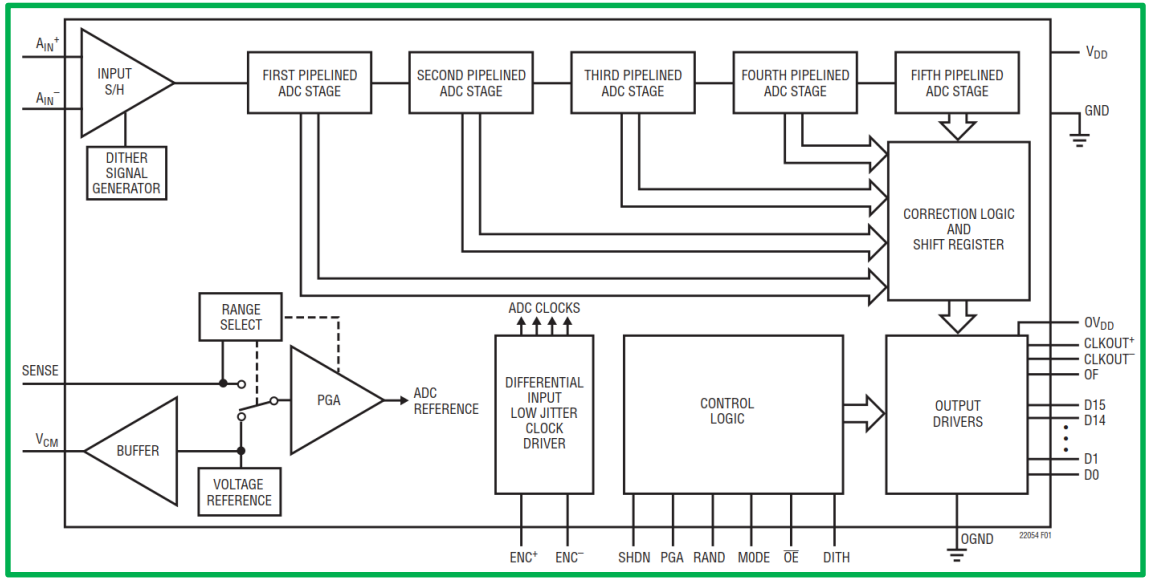


DDC Bypass Mode
F_{IN} = 2497.97 MHz at –7 dBFS
f_S = 4000 MSPS

Comparison


AVDD
VREFP
VREFN
DVDD
IOVDD
VCOM
R
R
VREF
Mod 1
Mod 2
Mod 8
Modulator Output
AINP1
AINN1
VIN1
ΔΣ Modulator1
Digital Filter1
AINP2
AINN2
VIN2
ΔΣ Modulator2
Digital Filter2
INP4/8(1)
INN4/8(1)
VIN4/8
ΔΣ Modulator4/8(1)
Digital Filter4/8(1)
SPI and Frame-Sync Interface
Control Logic
DRDY/FSYNC
SCLK
DOUT[4:1]/[8:1](1)
DIN
TEST[1:0]
FORMAT[2:0]
CLK
SYNC
PWDN[4:1]/[8:1](1)
CLKDIV
MODE[1:0]
AGND
DGND


Buffer
VIN+
VIN–
ADC
VCM
VCMO
VBG
RBIAS+
RBIAS–
REF
DEVCLK+
DEVCLK–
VCM CLK
Clock Sync
SYSREF+
SYSREF–
SYNC~/TMST+
SYNC~/TMST–
SYNC~
TDIODE+
TDIODE–
DDC
DDC Bypass
JESD204B Interface
Overrange Detection
Configuration Registers
SPI Interface
DS7+/NCO_2
DS7–/NCO_2
DS6+/NCO_1
DS6–/NCO_1
DS5+/NCO_0
DS5–/NCO_0
DS4+
DS4–
DS3+
DS3–
DS2+
DS2–
DS1+
DS1–
DS0+
DS0–
OR_T0
OR_T1
SCS
SCLK
SDI
SDO


AIN+
AIN–
INPUT S/H
DITHER SIGNAL GENERATOR
FIRST PIPELINED ADC STAGE
SECOND PIPELINED ADC STAGE
THIRD PIPELINED ADC STAGE
FOURTH PIPELINED ADC STAGE
FIFTH PIPELINED ADC STAGE
CORRECTION LOGIC AND SHIFT REGISTER
VDD
GND
RANGE SELECT
SENSE
VCM
BUFFER
VOLTAGE REFERENCE
PGA
ADC REFERENCE
ADC CLOCKS
DIFFERENTIAL INPUT LOW JITTER CLOCK DRIVER
CONTROL LOGIC
OUTPUT DRIVERS
OVDD
CLKOUT+
CLKOUT–
OF
D15
D14
D1
D0
OGND
ENC+
ENC–
SHDN
PGA
RAND
MODE
OE
DITH

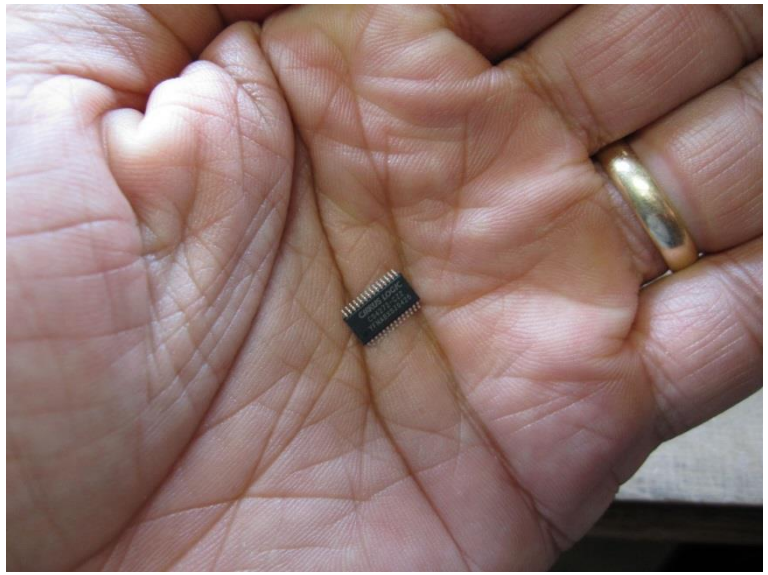
What is a nice ADC ?

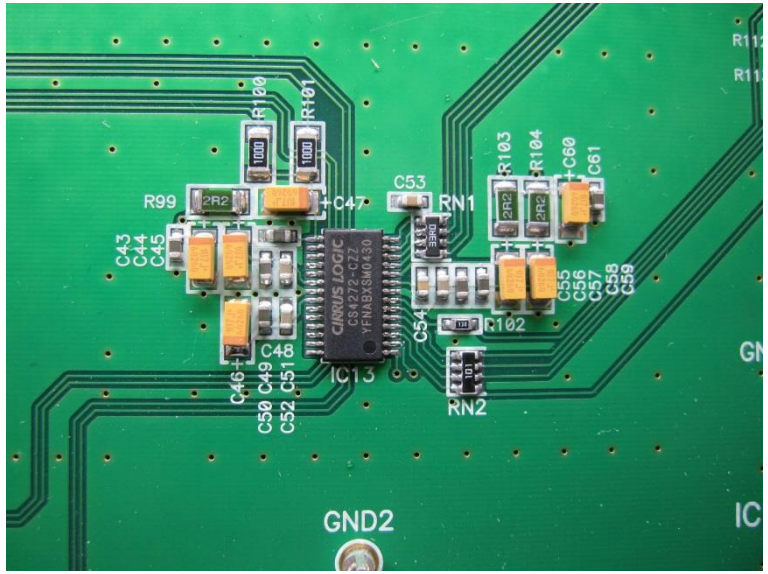
- Must have:
  - a good datasheet
  - good datasheet performance
  - possible to buy
  - a differential analog input
  - possibility to connect an external reference

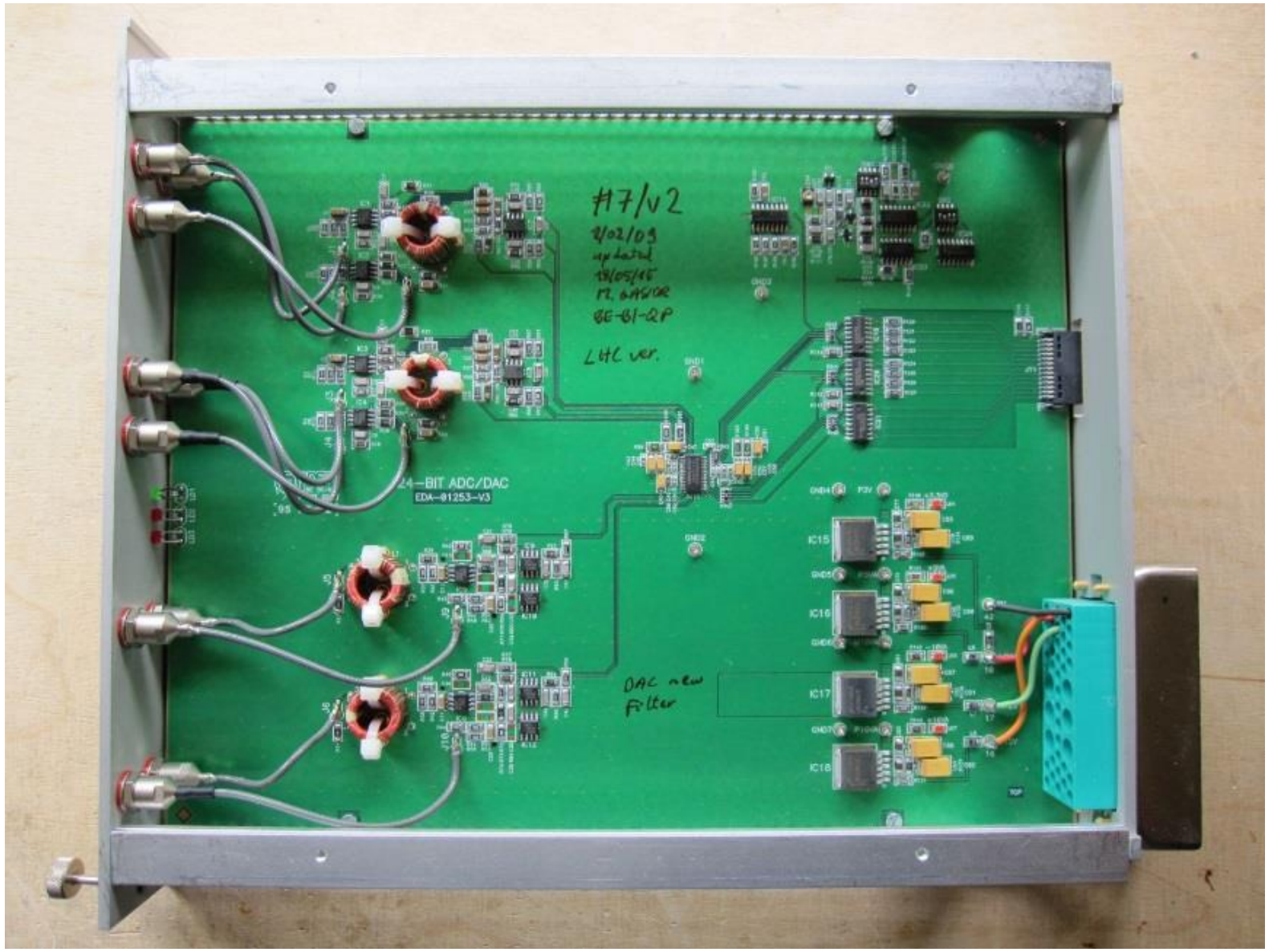
- Should have
  - development kit
  - simple interface to the external world

- Good to have
  - a few pin compatible versions with different sampling and resolution combinations
  - versions with different number of channels

ADC modules and boards

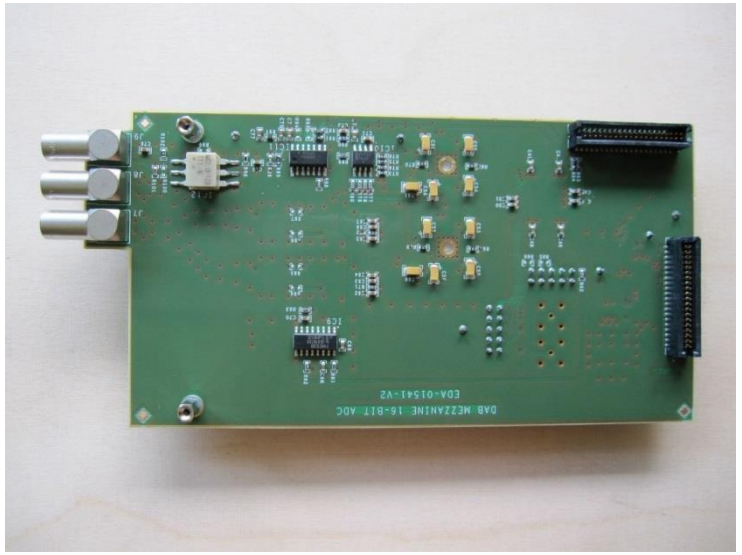


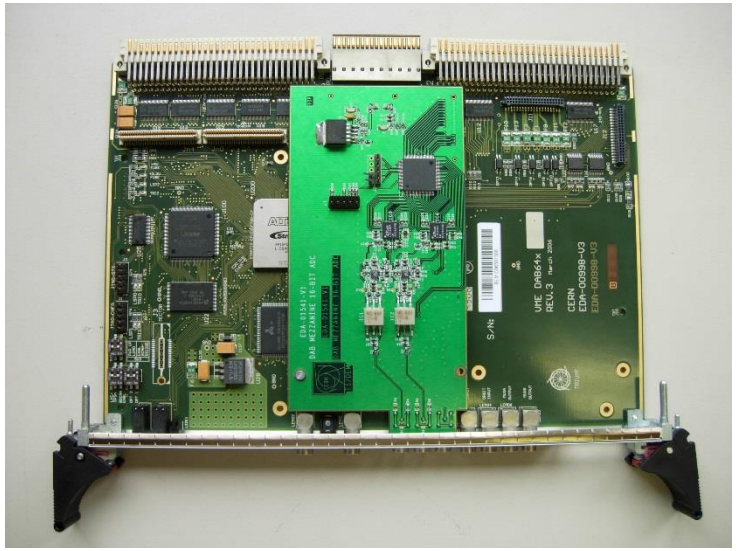


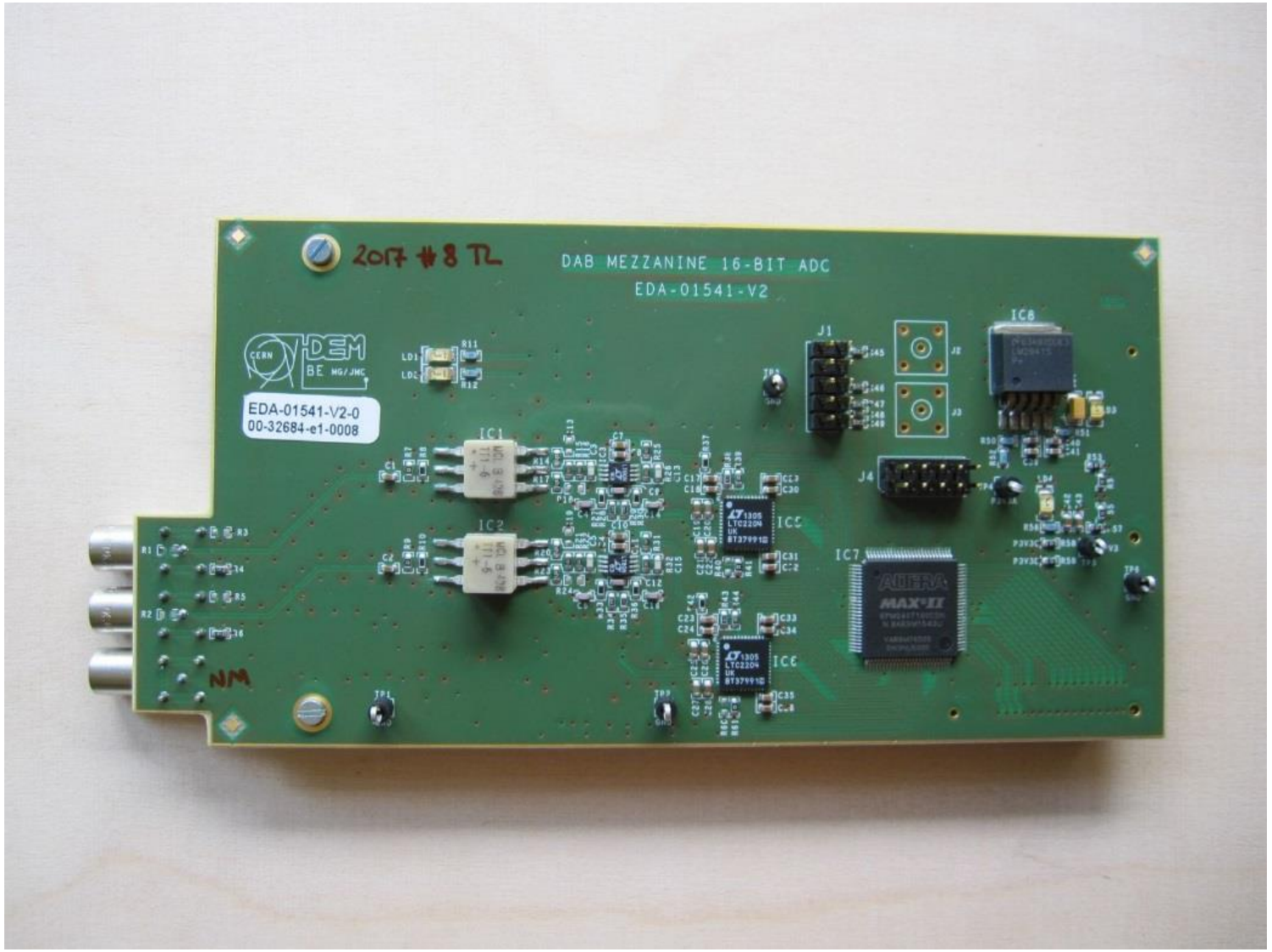


- Audio codec: 2 ADCs + 2 DACs, 24 bit, 192 kS/s, PCB: 4 layers, smallest component 1206 (3.2 × 1.6 mm)

ADC modules and boards

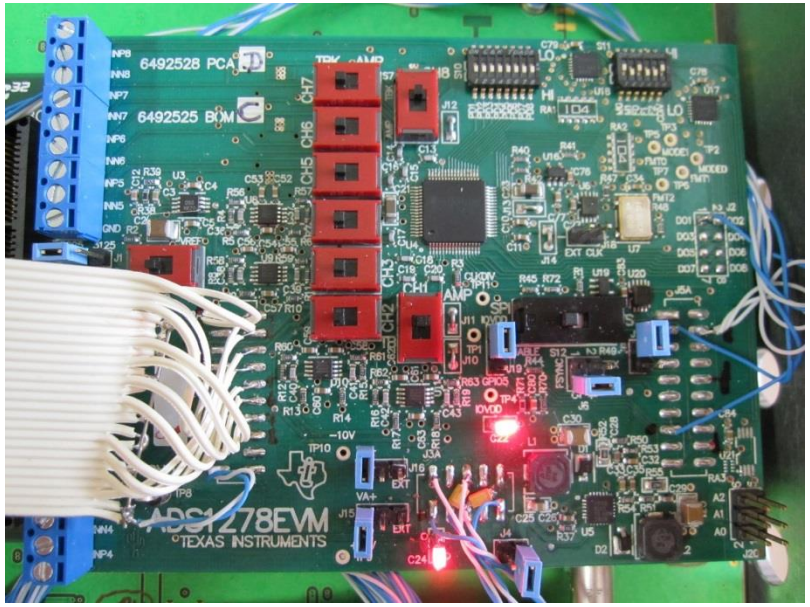


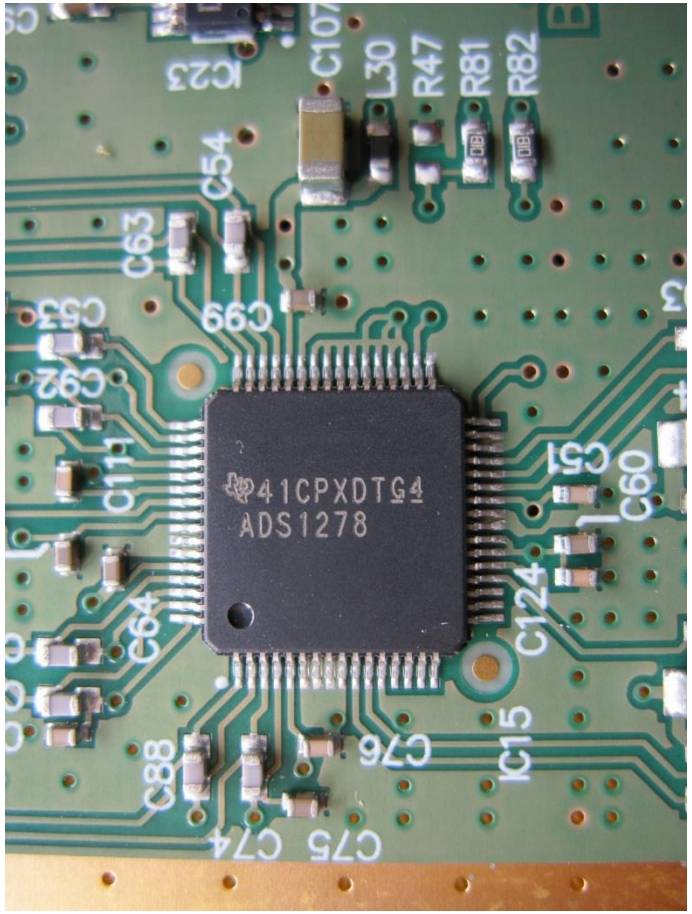


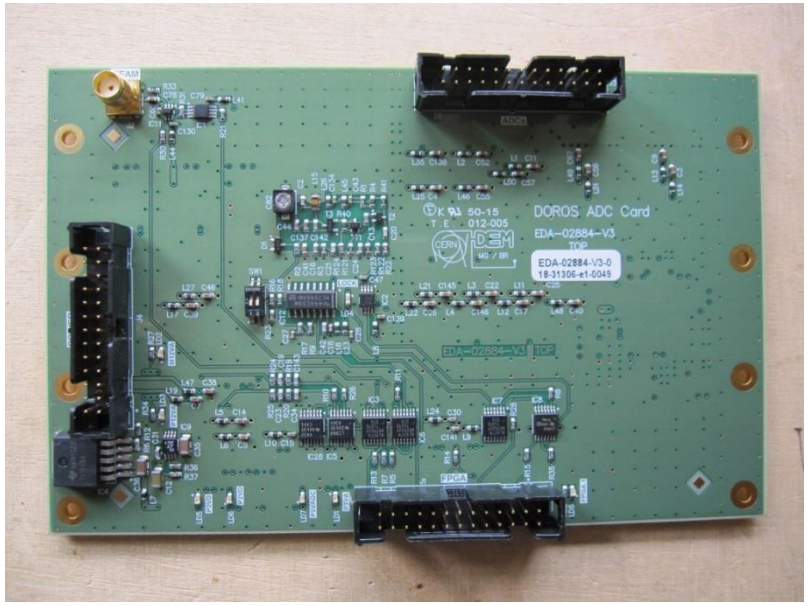


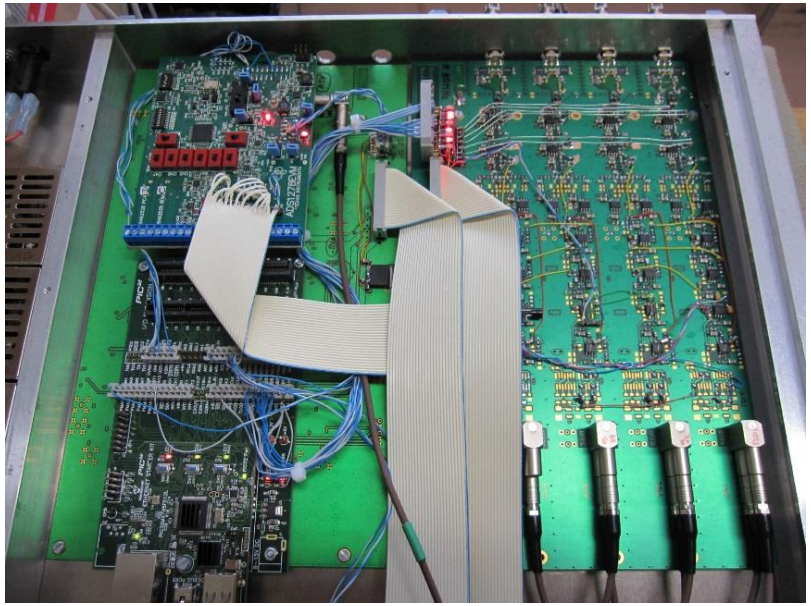
- PCB: 4 layers, smallest component 0603 (1.6 × 0.8 mm)

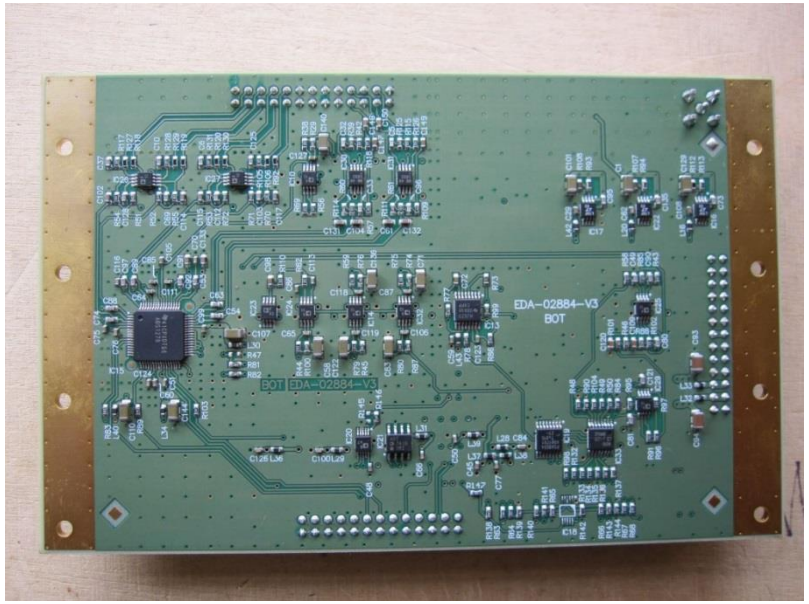
ADC modules and boards





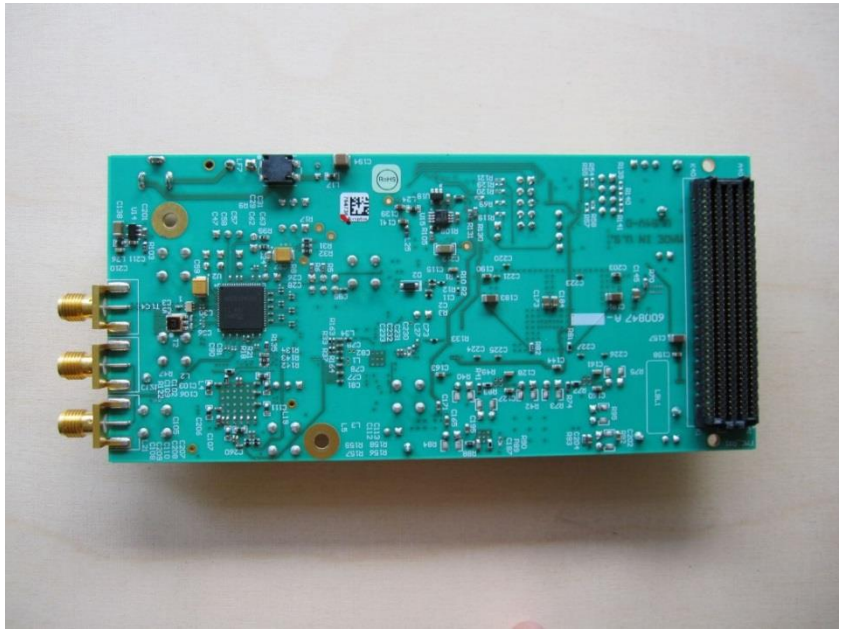


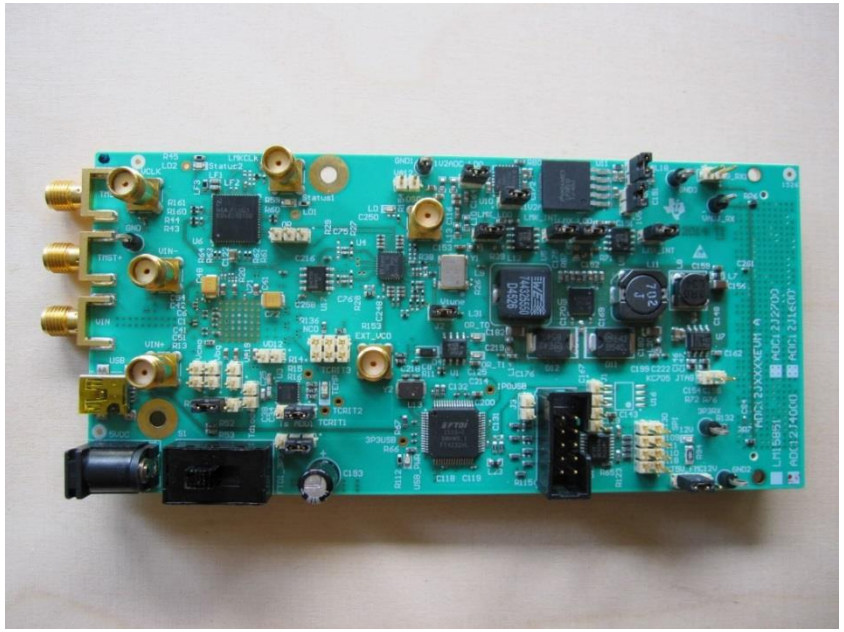


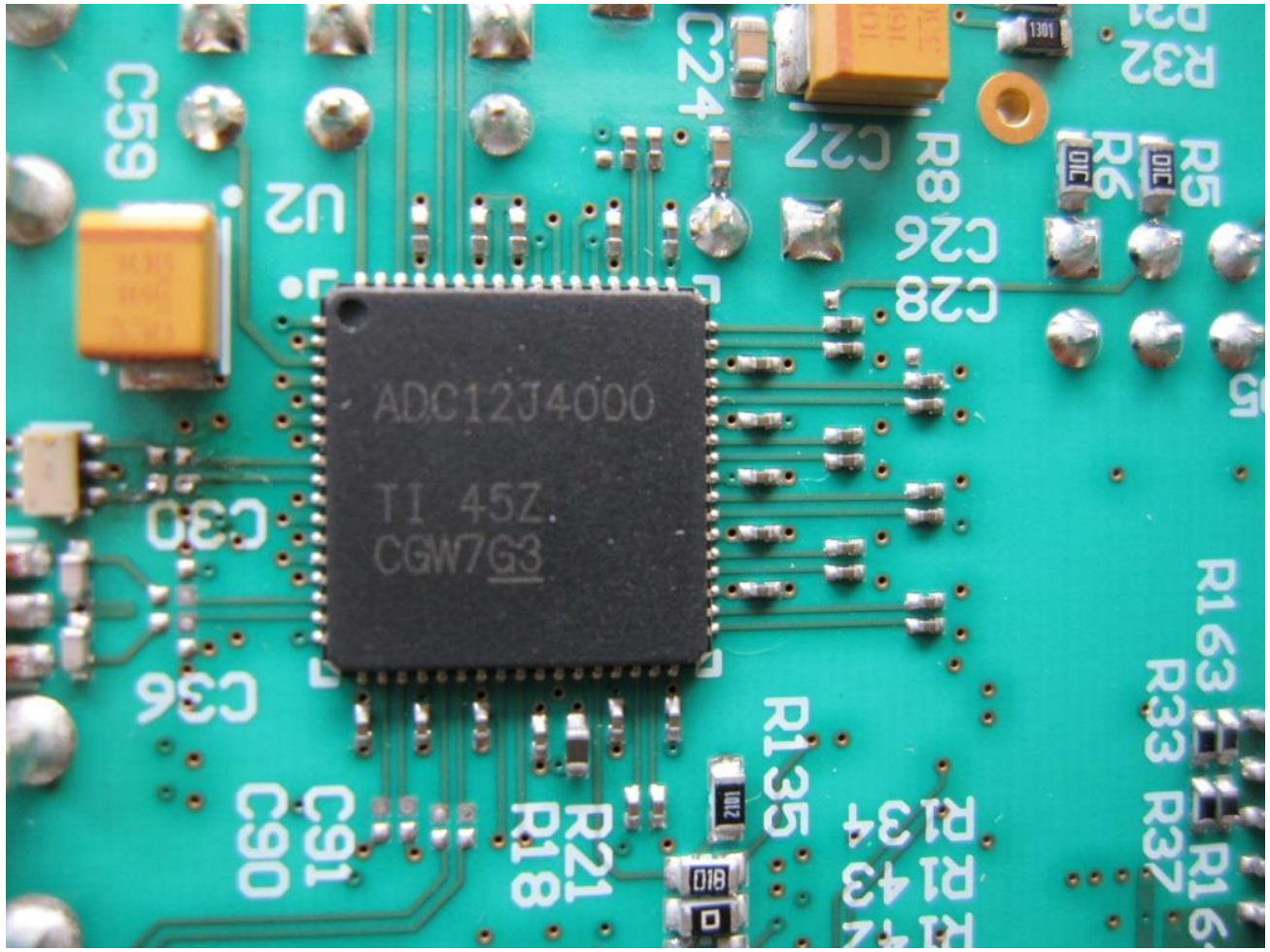


- PCB: 6 layers
- Smallest component 0402 (1 × 0.5 mm)

ADC modules and boards

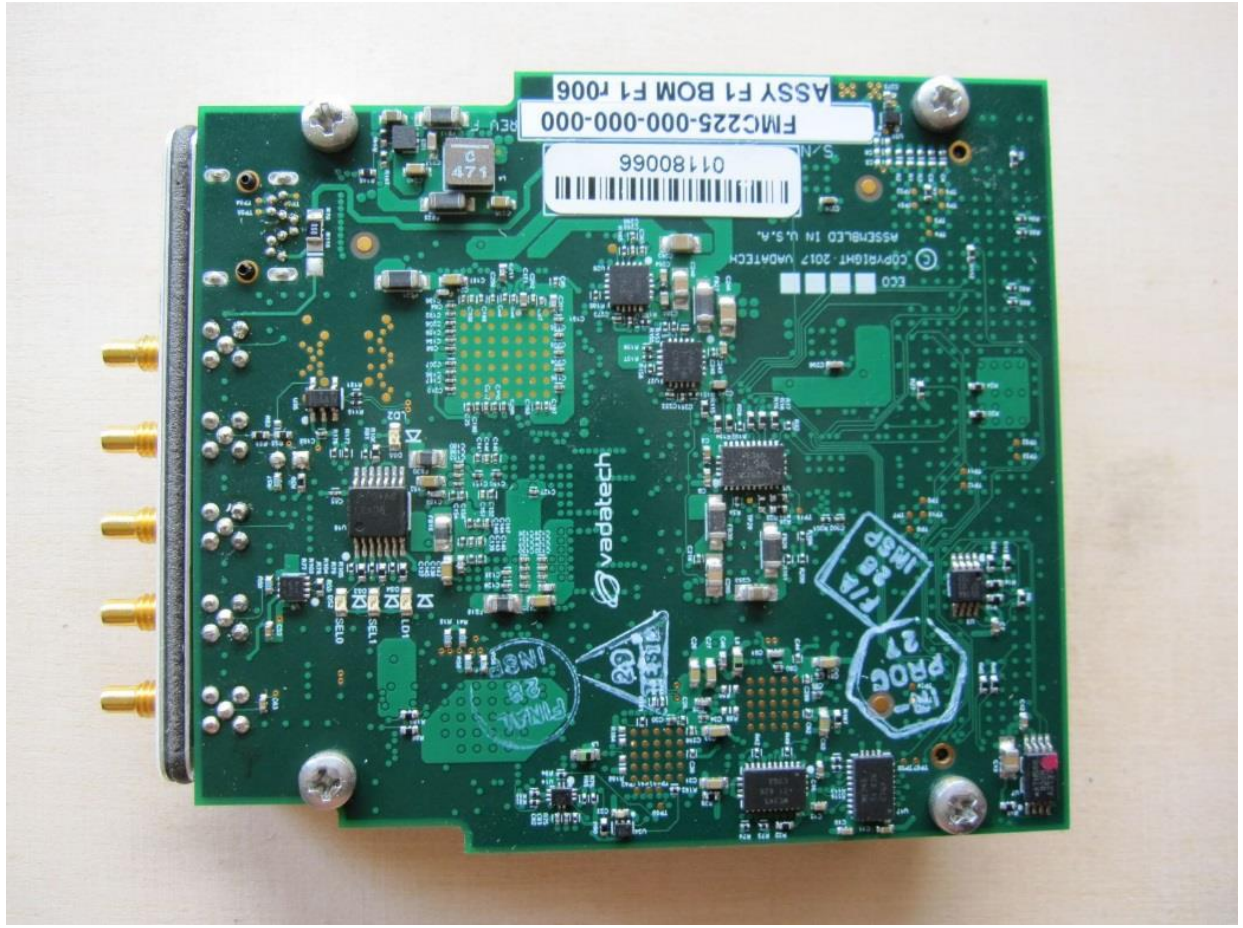


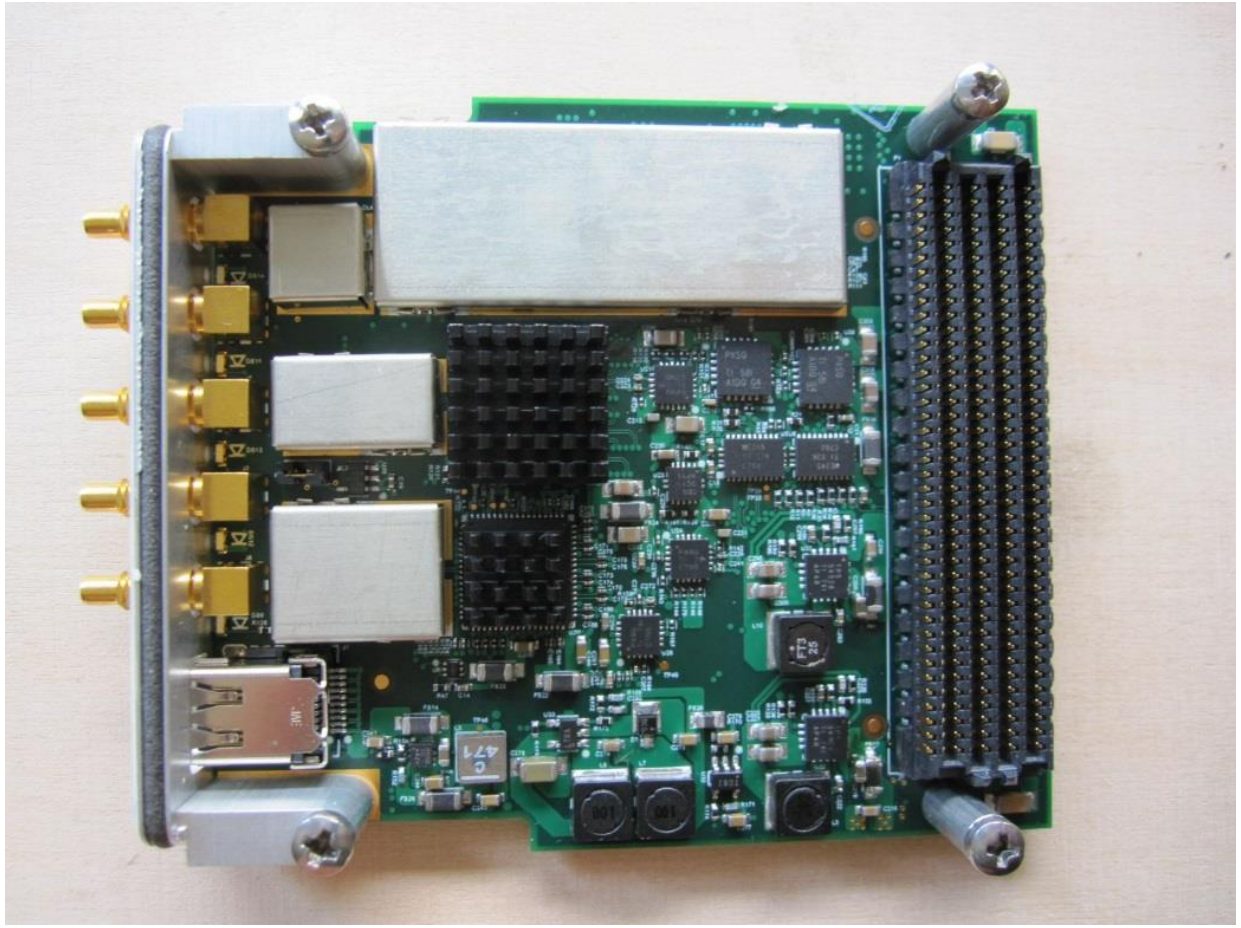




- PCB: smallest component 0201 (0.25 × 0.125 mm)

ADC boards/modules

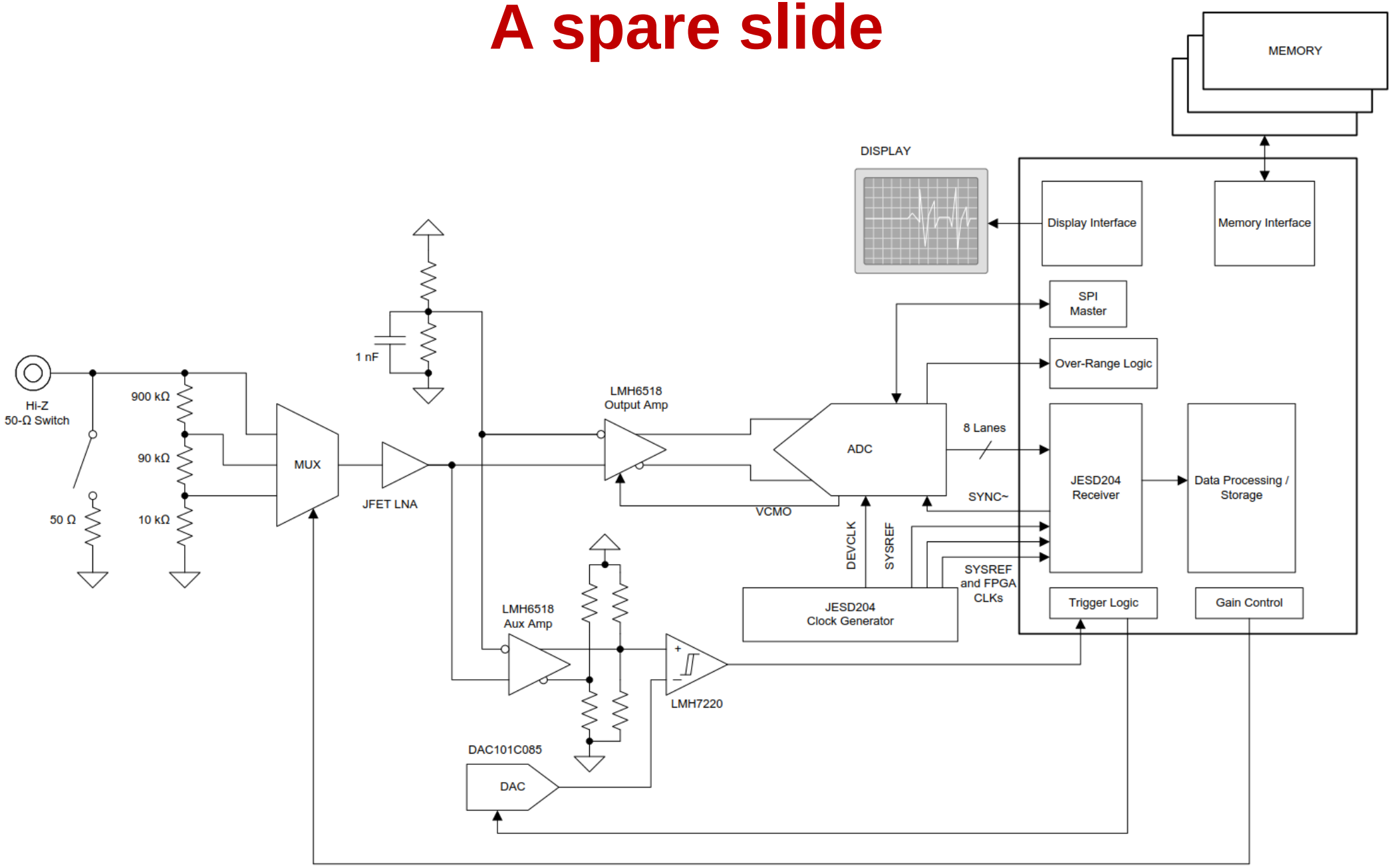




Summary

- General trend ”less analogue, more digital” makes the ADCs the key parts of BI systems
- Advancements in the ADC technology shifts the capabilities of BI systems, often at the expense of their higher complexity
- Nowadays high performance ADCs require quite complex “RF design” boards
- High performance ADCs need excellent external signals: clocks, references, power supplies, input circuits
- Do not underestimate the potential gain from good analog processing before the ADCs, especially for “difficult cases” = fast sampling and high resolution at the same time
- Detailed requirements for a new BI system are necessary to choose the optimal system architecture and an adequate ADC
  - time axis: a fixed clock frequency or a clock synchronised to a timing
  - amplitude axis: one dynamic range, a few ranges, a programmable gain control
- Slower sampling rates help for everything, except the time resolution: noise, distortion, data rate, power consumption, complexity, money, manpower
- The faster, the better: NOT TRUE, the more bits, the better: TRUE (but more expensive)
- Reading data sheets is good, measuring is better
- Playing with simulated data is good, playing with measurement data is better
- Playing with ADC development kits at an early stage of the system design may be very useful

A spare slide



Simplified Schematic for an Oscilloscope