

# Control System Integration

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# Accelerator Control System

- Conveys all monitor, control, model-based, and computed data from all accelerator, facility, safety, and operations subsystems to accomplish supervisory control, automation, and operational analysis.
- Scope extends from the interface of the equipment being controlled through to the designers and operators of the accelerator facility. Sometimes including experimenters
- Includes all hardware and software between these bounds: computer systems, networking, hardware interfaces, and programmable logic controllers
- Not restricted to closed loop control systems (a primary focus in this school). In fact, at some accelerator facilities, these systems are treated as black boxes developed by the technical groups.

# Responsiveness

Configuration  
Archiving  
Analysis...

Control Room  
Physics Apps...

Digital Signal  
Processing  
Subsystem

Office PC  
Network

Supervisory Control  
System (SCADA)

Fly by  
Wire

Nodes are responsive  
Network is responsive

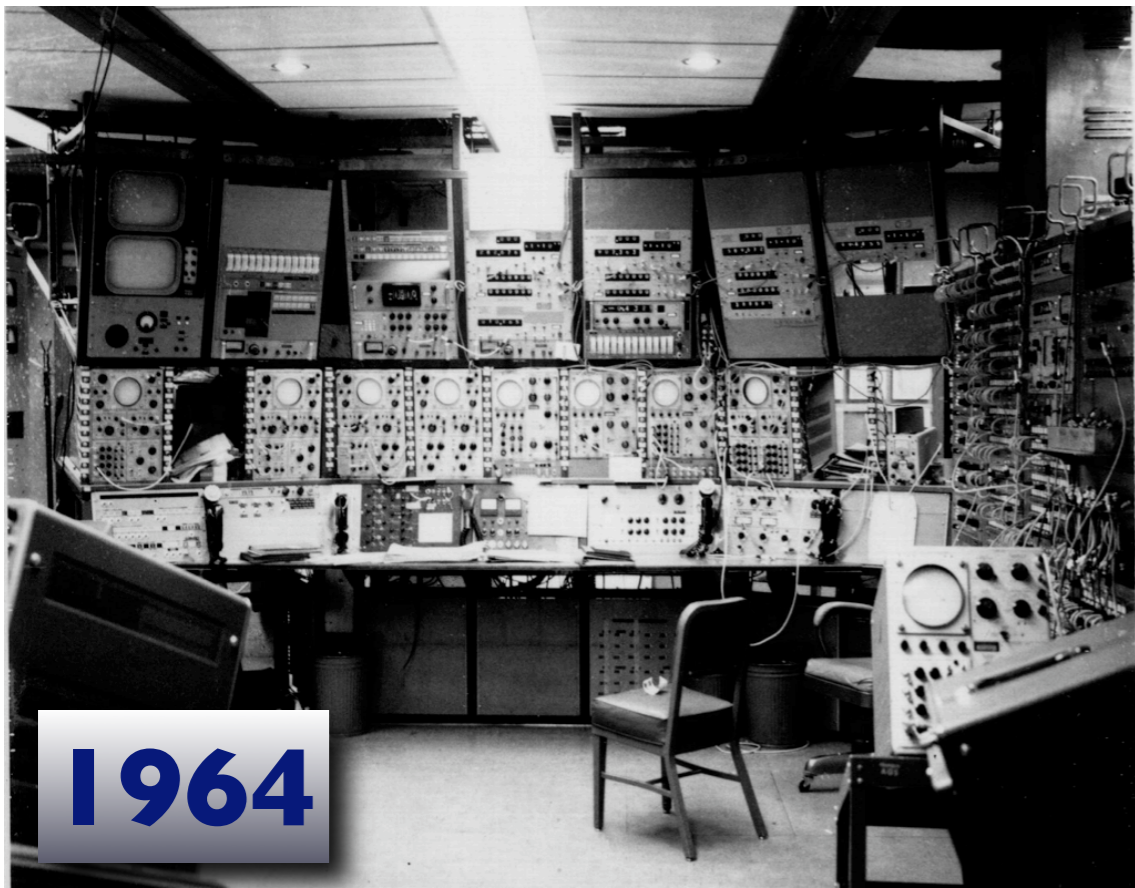


Nodes are real-time  
Network is responsive



Nodes are real-time  
Network is real-time





**1964**



**1989**



**1998**



**2006**

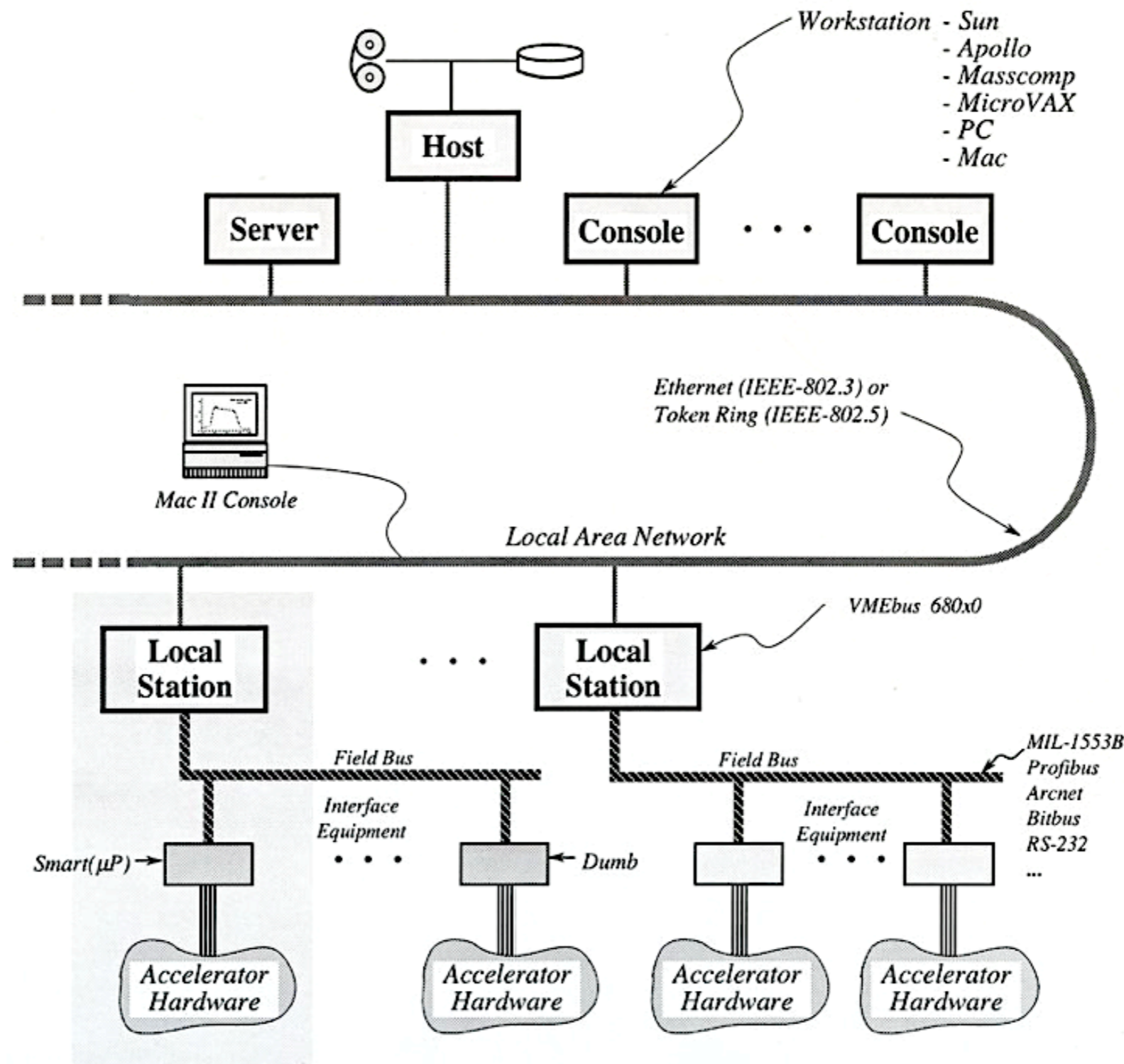


# Out With the Old, In With the New, circa 82



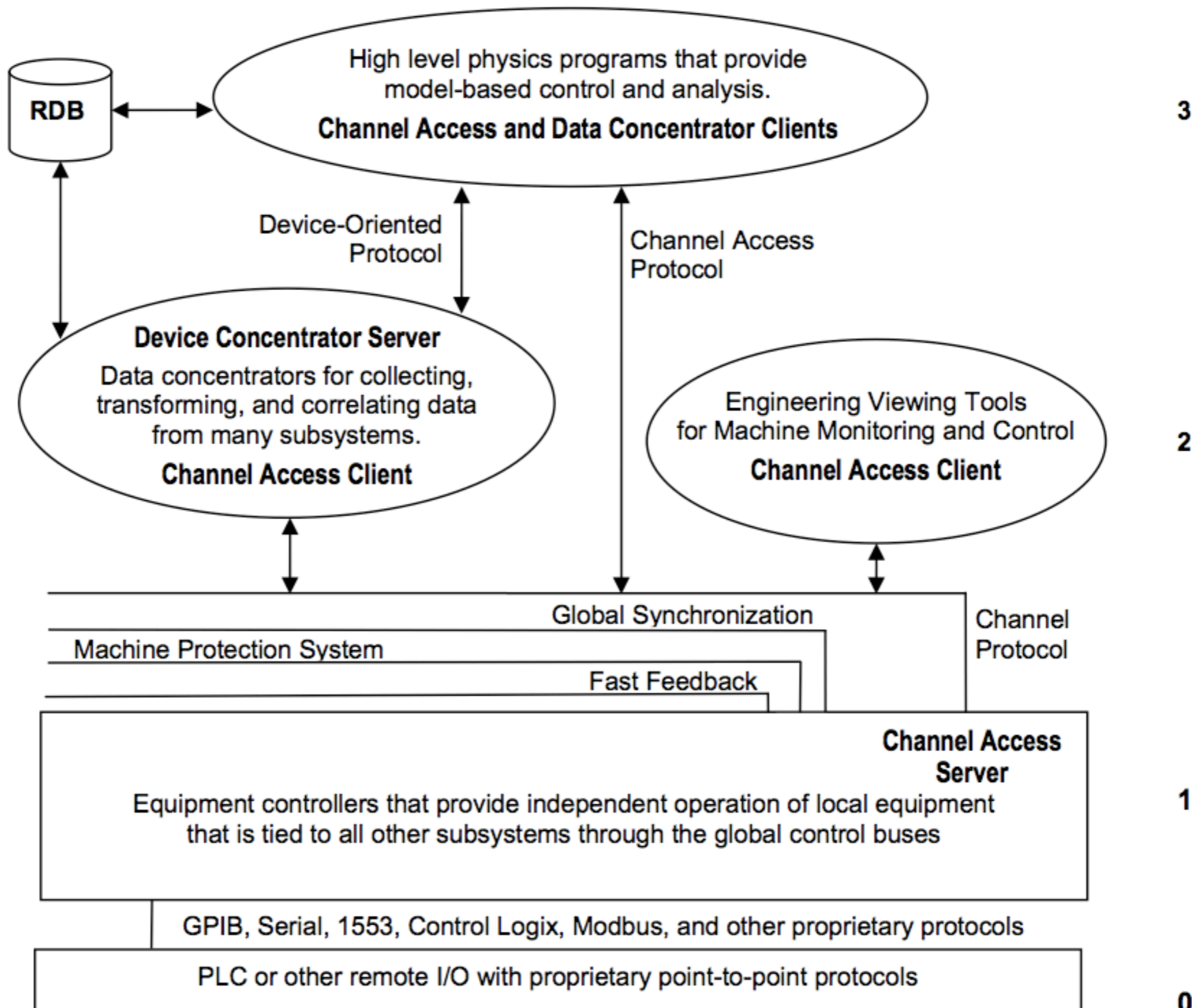


# The "Standard Model"



Generic Distributed Control System Architecture

# Recent Example





# Evolution of Distributed Systems

- mainframe/VAX
  - limited I/O drops lead to long analog signal runs
  - Centralized computing resources
- Standard Model
  - distributed I/O controllers
  - shorter analog runs
- Refinements to standard model
  - NAD: finer grained distribution
  - Multi-Tier/Middleware
  - New platforms: ATCA, etc...

# Functional Interfaces

## Communications

- Backplane (Internal)
- Network
- Real-time data\*
- Event\*
- Reference Clock\*\*
- Machine protect\*
- Utility\*
- Beamline Device I/O\*\*\*
- Power
- Environmental

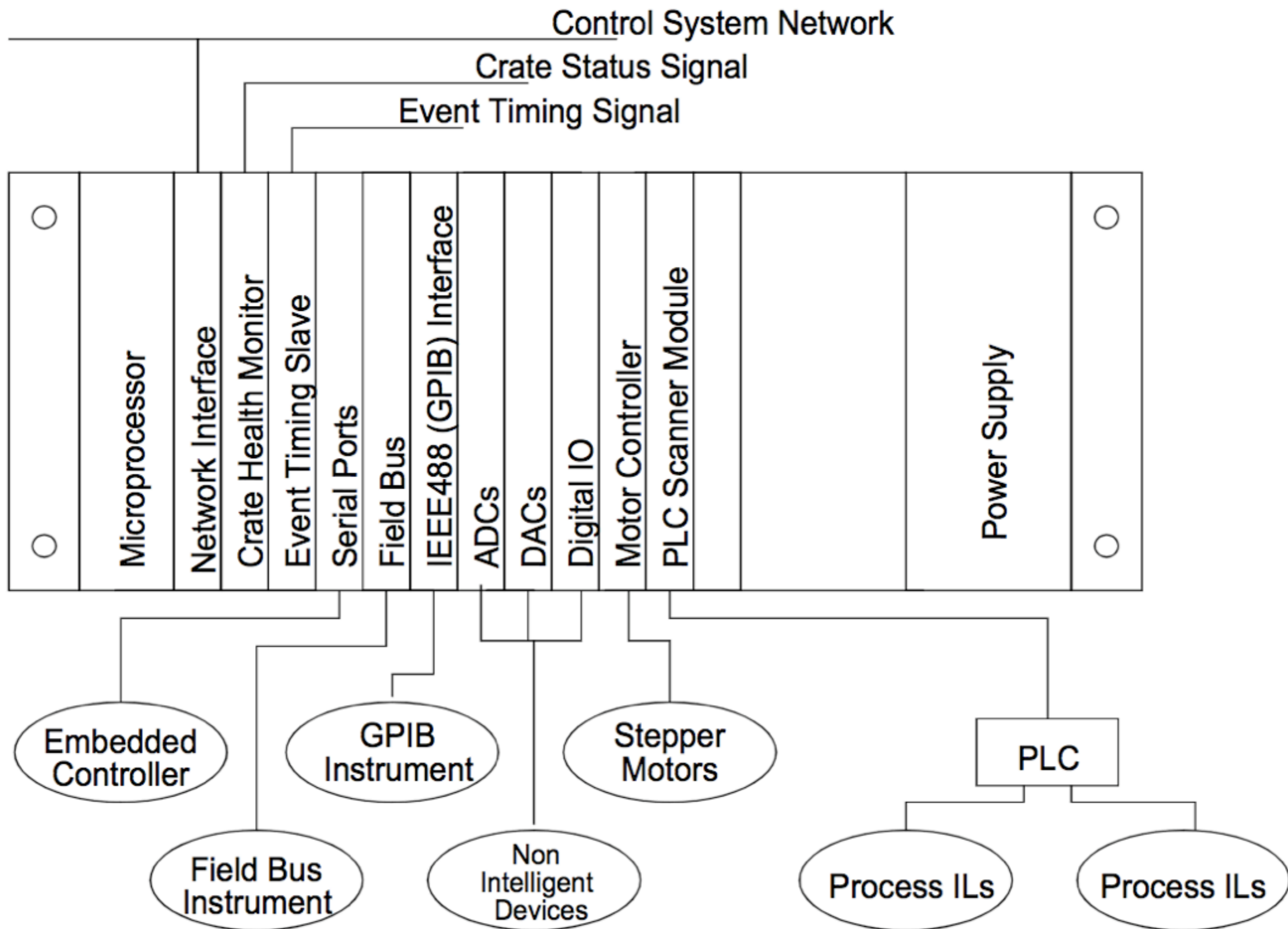
Typically specific to:

\* facility

\*\* machine

\*\*\* device

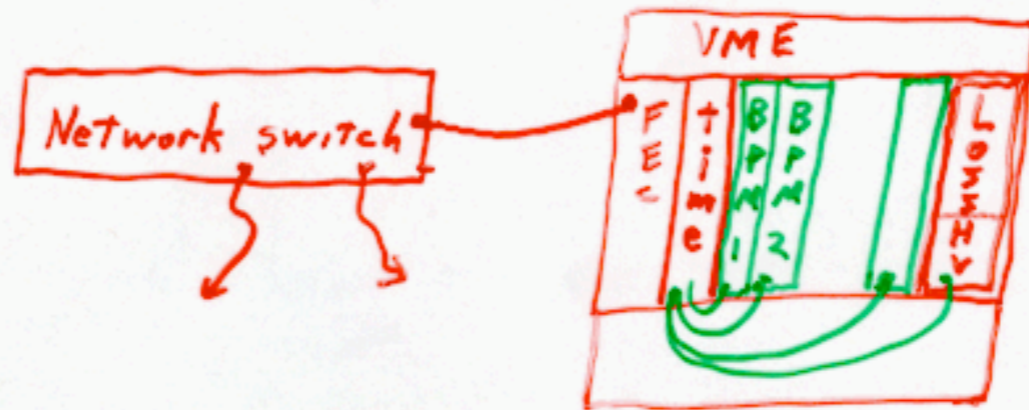
# Typical Crate



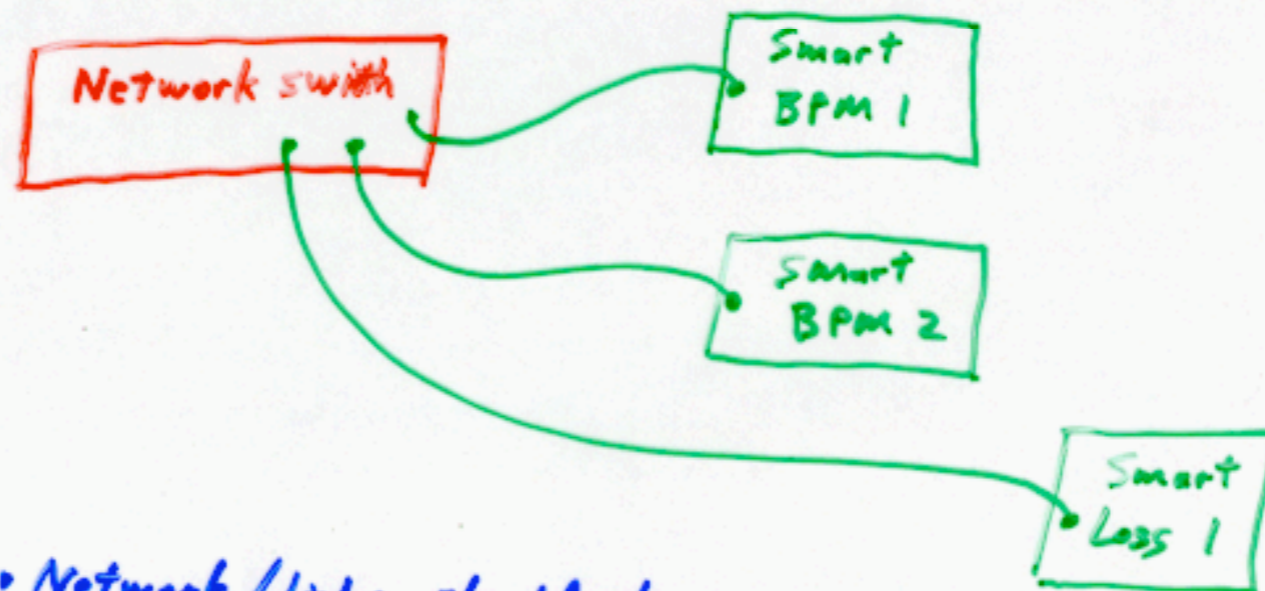


# Toward Network Attached Devices

Old:



New:



- Network/links should become redundant
- Smart boxes should share common platform

Once upon a time, there were transparencies...

# Motivation for NAD

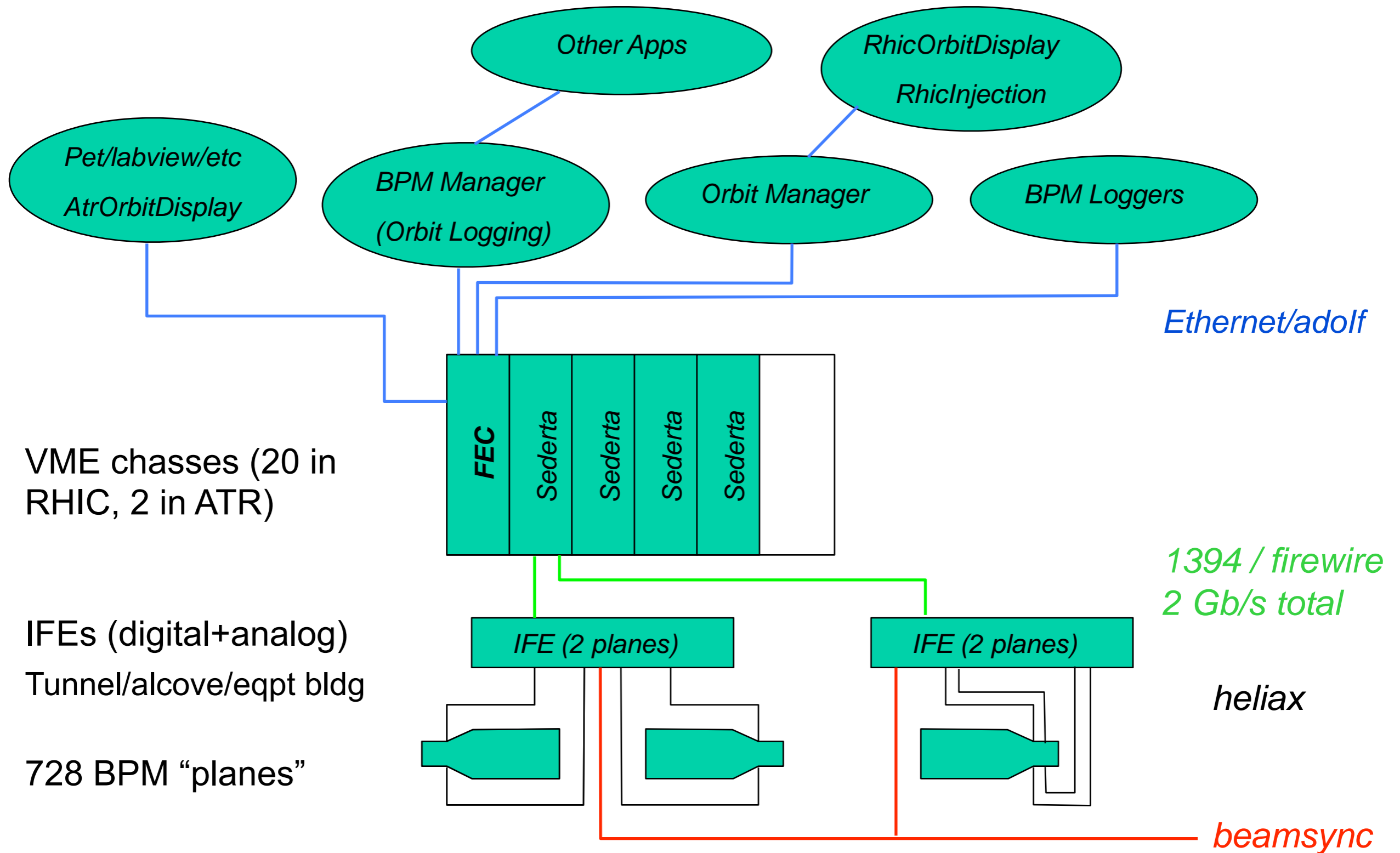
- **Shared resources** - tightly coupled
  - Tempting to make efficient use of modular infrastructure: pack with channels or share with multiple system types
  - System integration becomes more complex
- **NAD** - loosely coupled
  - limit unnecessary coupling between systems
  - vertically test individual units
  - integrate single units with focussed, well defined interfaces
  - Rapid SNS integration demonstrated success
- Even a subset of the concept can be helpful:  
i.e. get the mission critical vacuum interlock boards out of the experimental diagnostic crate, or integrate timing decoder on acquisition board in ATCA module

# Middleware

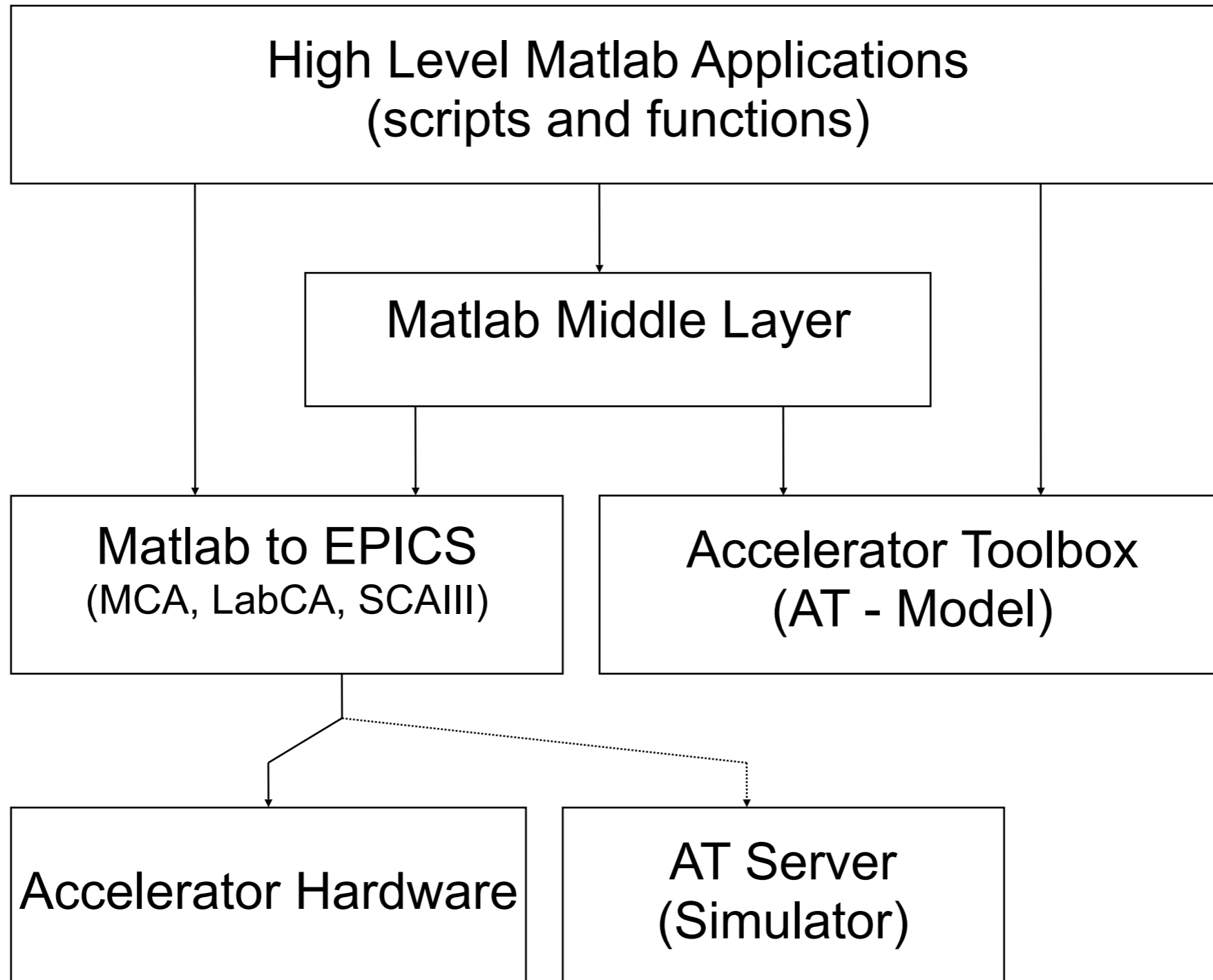
- Glue
- From component/device view to physics view
- Uniform access to multiple information sources (front end computers, online model servers, databases...).
- Could be soft real-time
- Complete solutions used heavily in the financial industry, less so in accelerators (but watch LHC)
- But many purpose-built implementations in use:
  - adapters
  - aggregators of requests (multiple clients) or responses (device collections particularly to support distributed high channel count systems)
  - correlators



# RHIC BPM System Overview



# Matlab MiddleLayer



# Physical Packaging

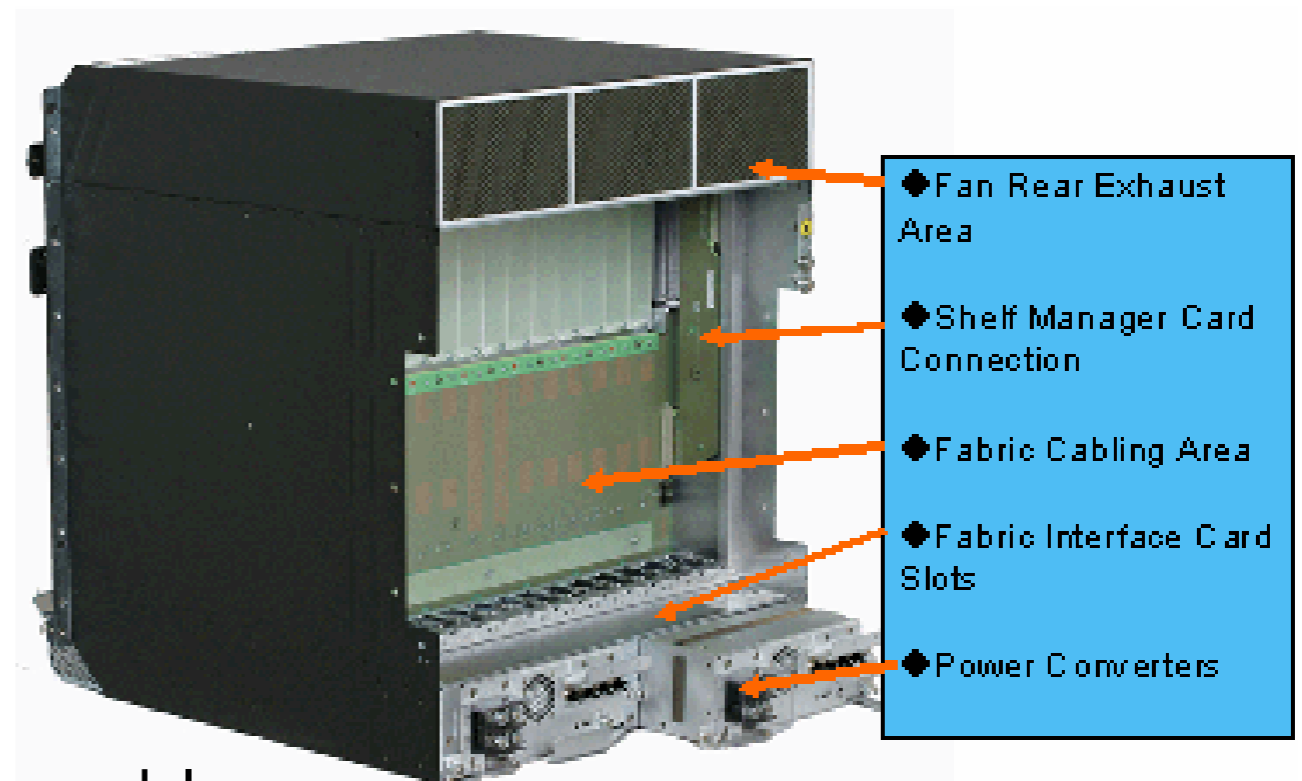
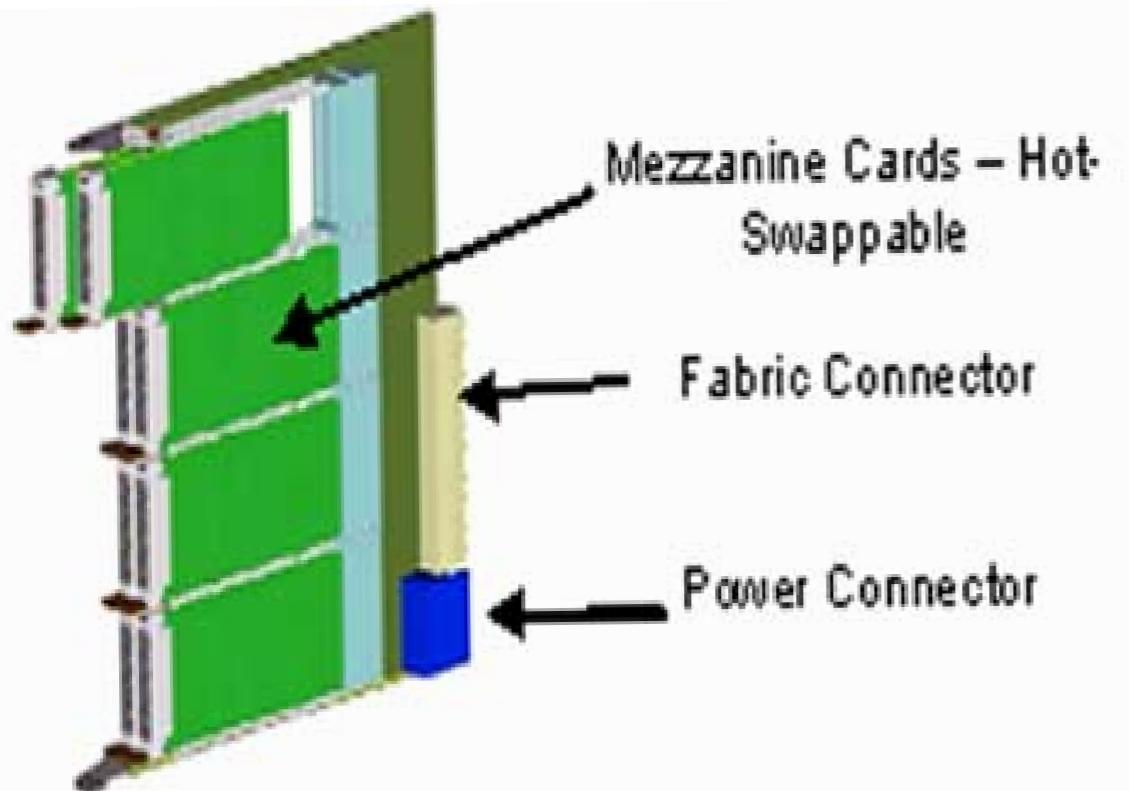
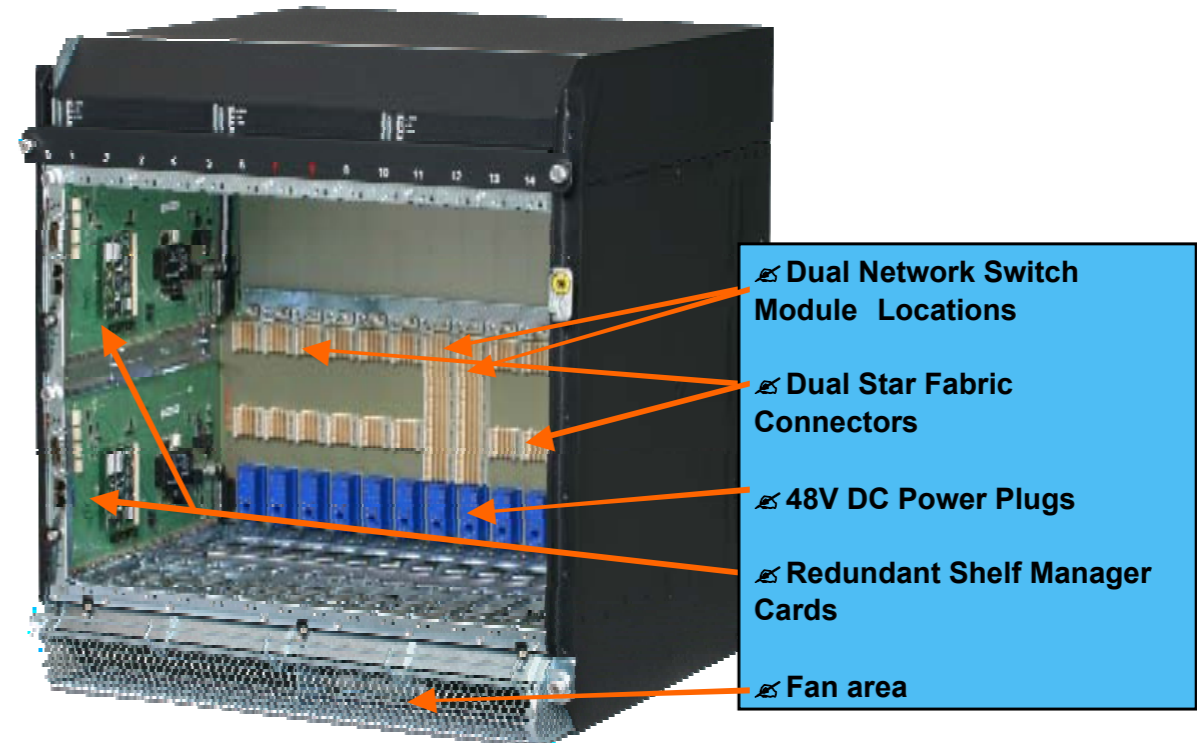
- Field replaceable units can be:
  - Modular
  - Self contained - i.e. rackmount, wall mount
  - Integrated - i.e. PS controller

# Packaging issues

- Power
- Cooling
- Shielding
- Connections
- Partitioning
- Standardization
- Availability/MTTR

# Modular Packaging

- VME/PCI/cPCI
- VXI/PXI
- ATCA (shown)



Best MTTR with I/O on rear transition module



# Self contained

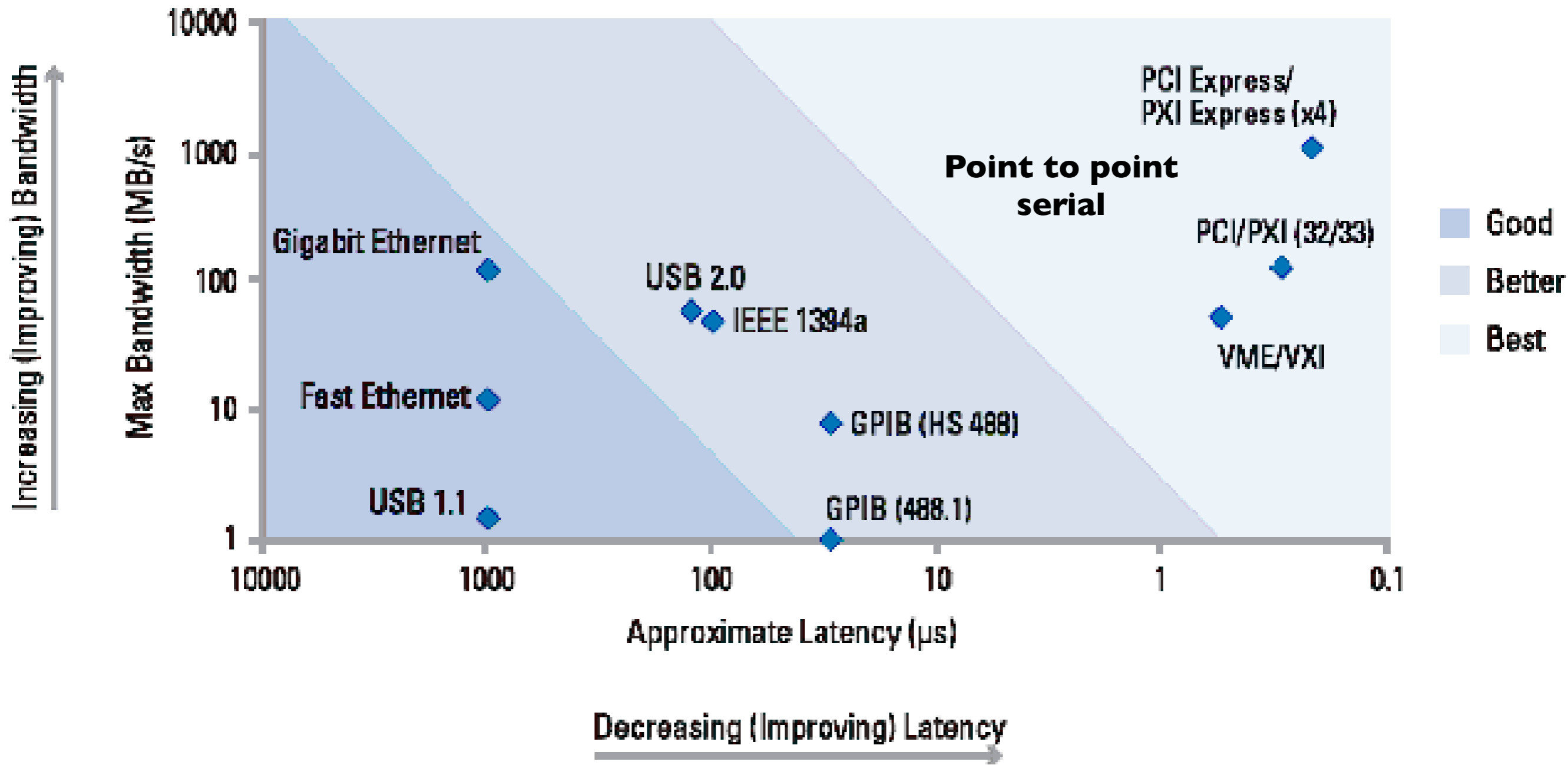
- Rack mount industrial PCs acting as NADs
  - could choose to stock prebuilt units as spares
  - changing I/O boards could lead to higher MTTR
- Chassis containing more integrated electronics
  - RHIC BPM (19" rackmount - in house)
  - Libera (19" rackmount - vendor supplied)

# Communications

# Communications Trends at Accelerator Facilities

- End of traditional parallel backplane bus paradigm (Announced every year since ~1989)
  - VME-PCI still there
  - watch PCI Express, RapidIO, ATCA
- Commercial networking products
  - DAQ 94' Conference: ATM, DS-Link, FibreChannel, SCI
  - Today: Gigabit Ethernet (1, 10, 30 GB/s)
- The ideal processing / memory / IO bandwidth device
  - The past: Transputers, DSPs
  - Today: FPGAs - Integrates receiver links, PPC, links, PPC, DSPs, memory.....
- Point-to-point link technology
  - The old style: Parallel Copper –Serial Optical
  - The modern style: Serial Copper –Parallel Optics, >3Gb/s today, 10Gb/s in demonstration

# Latency and Throughput



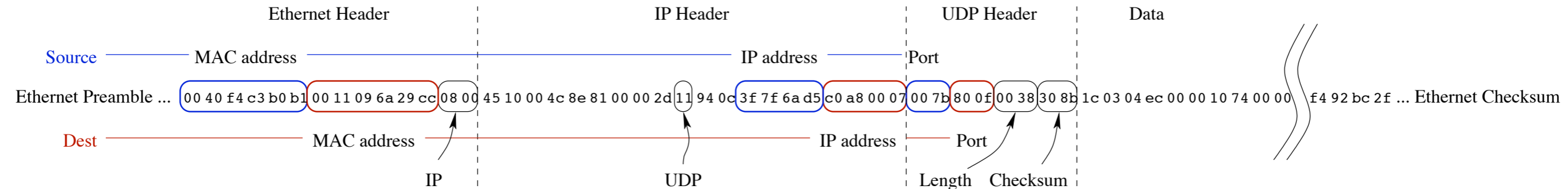
# Intra-chassis Standards

- CAMAC
- VME/VXI
- PCI/PXI
- IP, PMC
- PCIe
  - multilane serial
- ATCA
  - serial fabric
  - PCIe, ethernet, etc

	ATCA	PCI (long)	VME 6U
Board Area cm <sup>2</sup>	995	316	373
Power Watts	200	10/25	30
Bandwidth I/O Gb/s	20 full duplex	4.3 66MHz 64 bits	2.4 VME 2eSST
Front panel H * W cm	30 * 2	8 * 1.2	21.5 * 2
Component Height mm	21.33	14.48	13.72

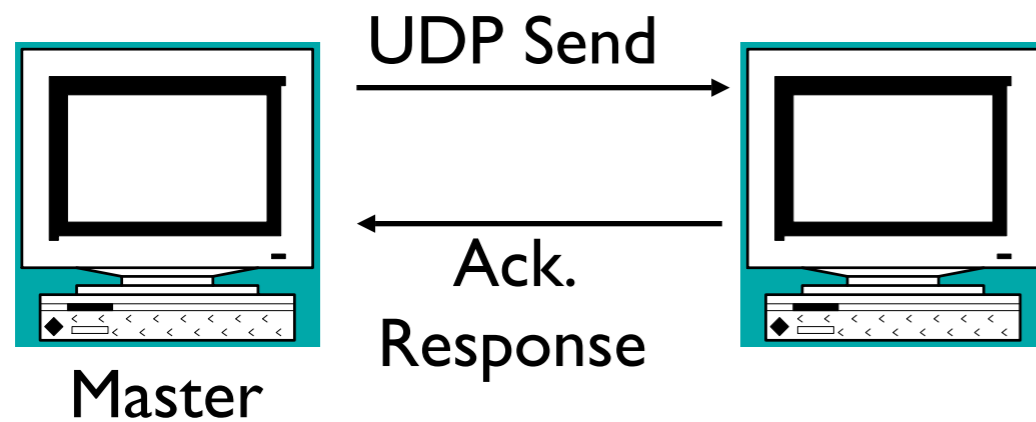


# UDP over Ethernet

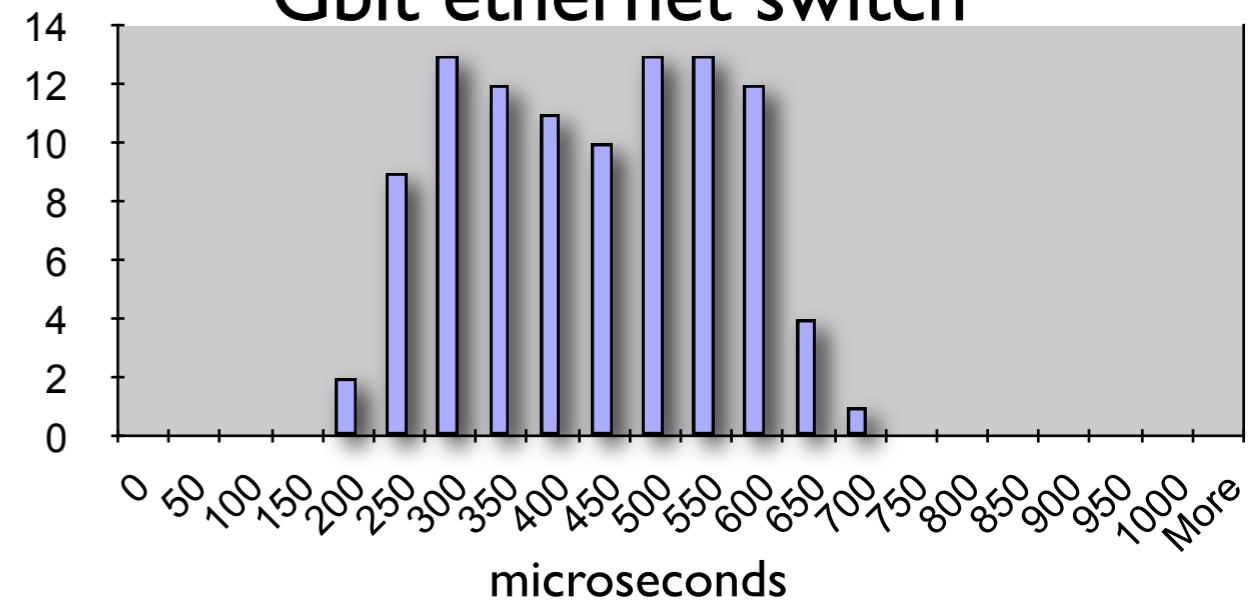


- TCP: http, EPICS Channel Access
- UDP: deterministic communication, streaming multicast
- Either one: COTS routers, diagnostic tools
- intended for implementation with processor, but simple UDP demonstrated in hardware

# Latency test for user mode process

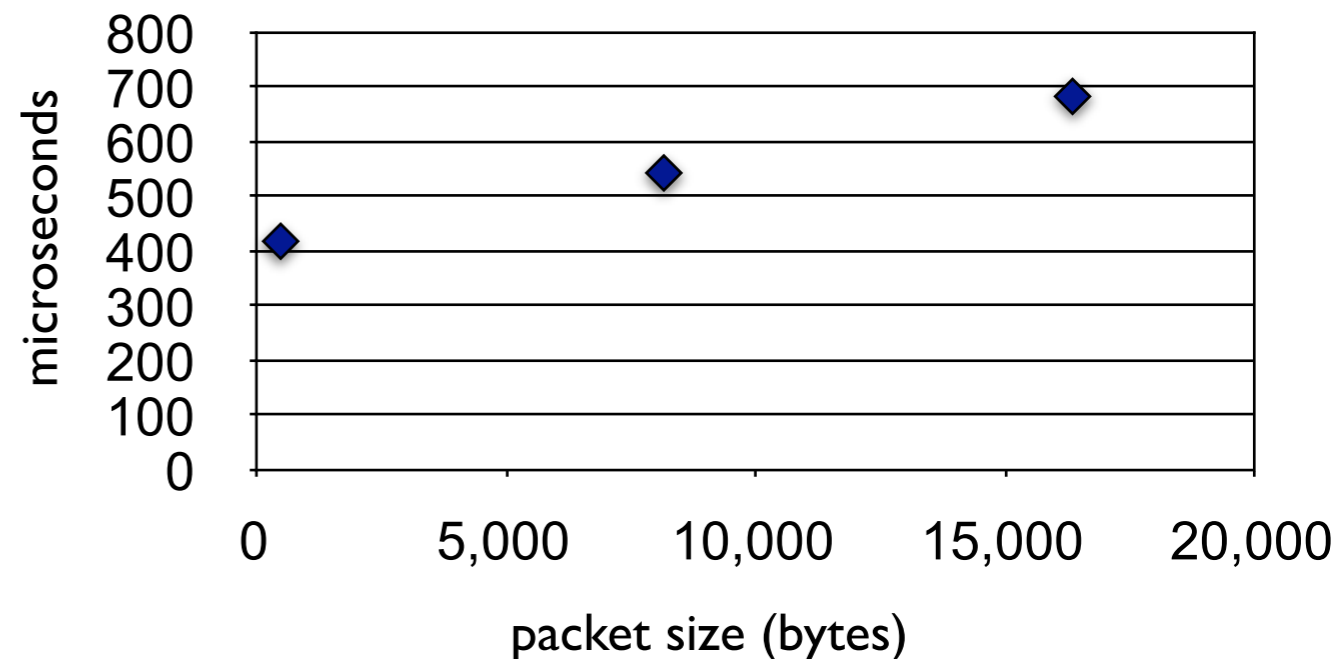


Round Trip with 2005 vintage Tyan, Gbit ethernet switch



Measure time difference  
UDP Send – Ack Response  
At Master using high res. timer

300usec round trip latency.  
one hit at 1.7msec  
Point to point, no switch  
2002 Vintage Dell running  
Standard Windows 2000

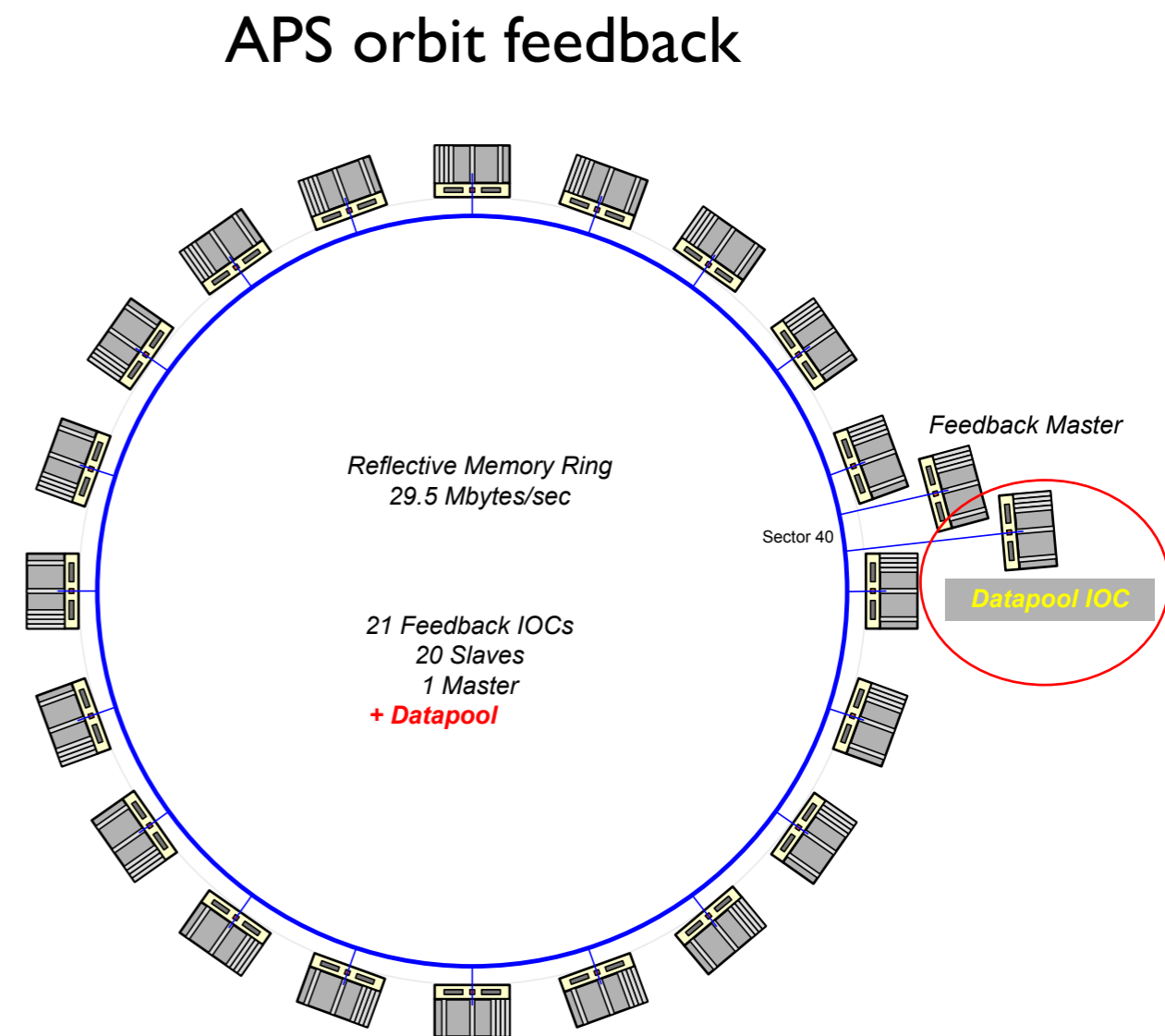


# Response Time

- What affects response time?
  - Network collisions (use switches/synchronization)
  - Thread Quantum (improved with preemptive interrupt capable OS: RTOS, Solaris, Windows, and new Linux Kernels  $\geq 2.6$ )
  - Context Switching times (10usec-100usec)
  - Packet size (Minor for small packets)
- Example using RTOS:
  - ALS orbit feedback system demonstrates negligible effect of UDP packet jitter @ 100Mb/s. Currently 1.1kHz rate. Expect to achieve 5 kHz rate @ Gb/s

# Reflective Memory Example

- Also known as Replicated Memory
- Each participant in the reflective memory network has a reflective memory module.
- Each module can be written and read as simple memory
- Property:
  - Anything written to a location in one reflective memory module appears (after a loop transit time) in the same location in all attached modules.
  - Transfer rate 29.5 Mbytes/second
- All Nodes see the same memory image
- Designed for Real-time Performance – Latency is minimized
- Typical implementation: Commercial PMC card on VME carrier or VME CPU board
- Calculated loop settling time = 21.4 usecs (22 nodes and 1200 meters of fiber)



# Timing/Event Systems

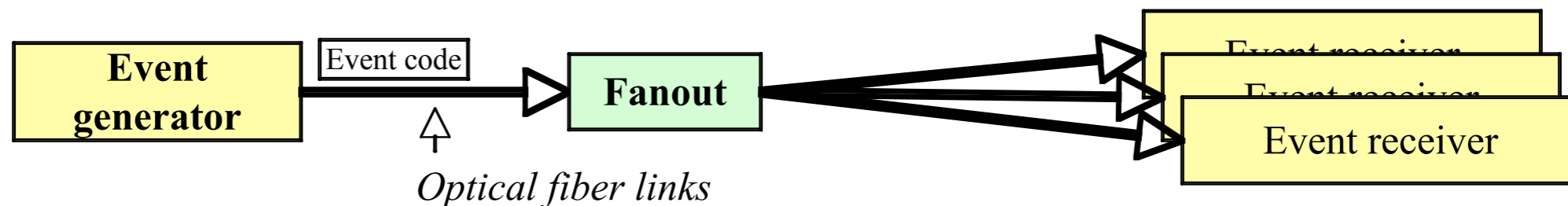
- Functions:
  - Coordination of actions
  - Correlation of data
- Other aspects to consider:
  - Multiuser operation
  - Frequency change if beam synchronous
- Scalability: information should reach ALL devices
- Implementations
  - FNAL/AGS/RHIC/SNS separated function
    - Event Link, TClock
    - RTDL, MDat
- SLS, Diamond: Events/info on Ethernet PHY
- Other options
  - UDP broadcast
  - Direct fiber
  - “tagged” RF reference clock



# Typical Event System

The system provides:

- global distribution of events to all systems that have a receiver
- trigger and gate signals to hardware
- synchronized timestamp facility
- software sequencing by triggering channels to process from events
- software can be used to send events



The stimulus to send an event can be:

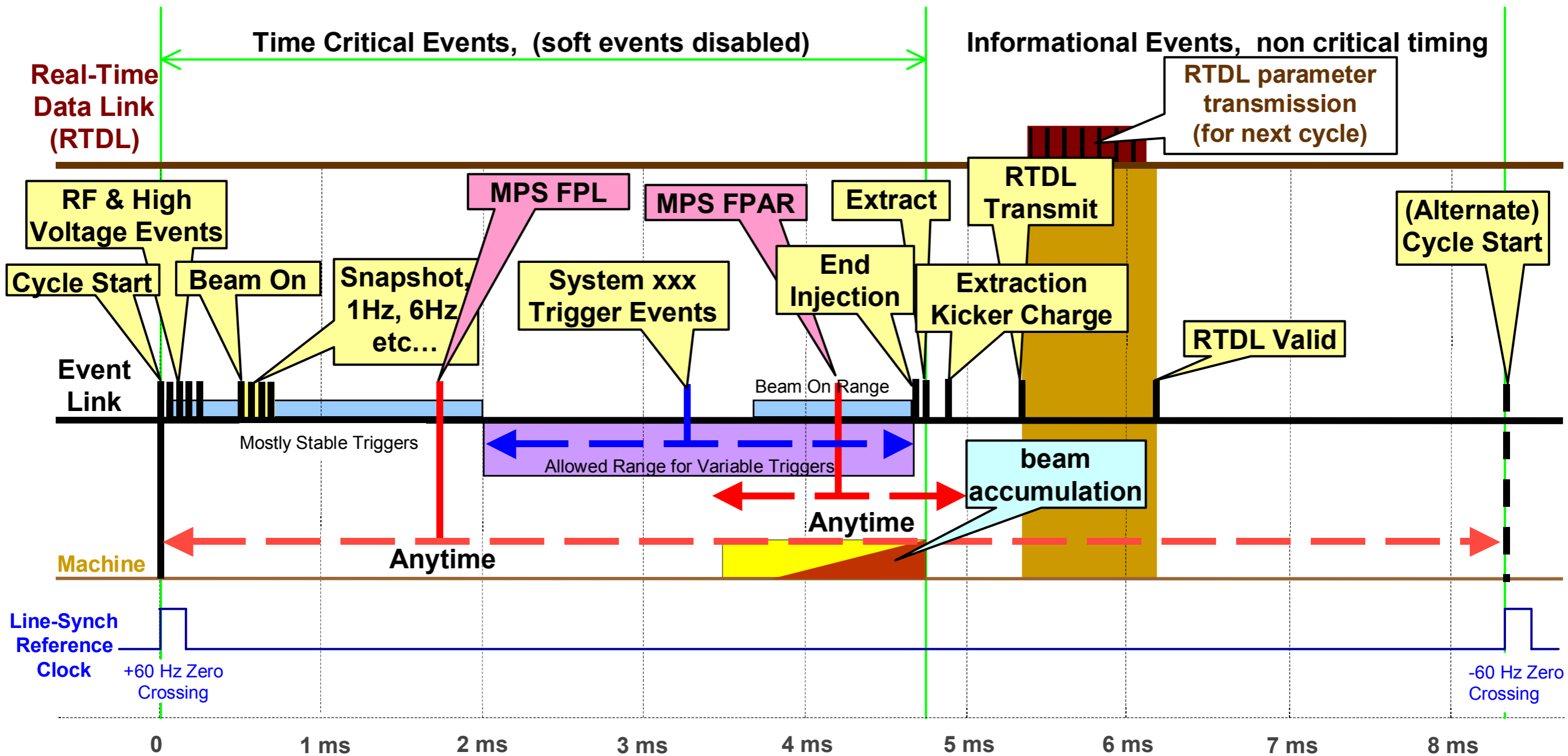
- pulse on a hardware input
- software event (write to a register)
- an entry in an event playback RAM .

When an event code is received the receiver can:

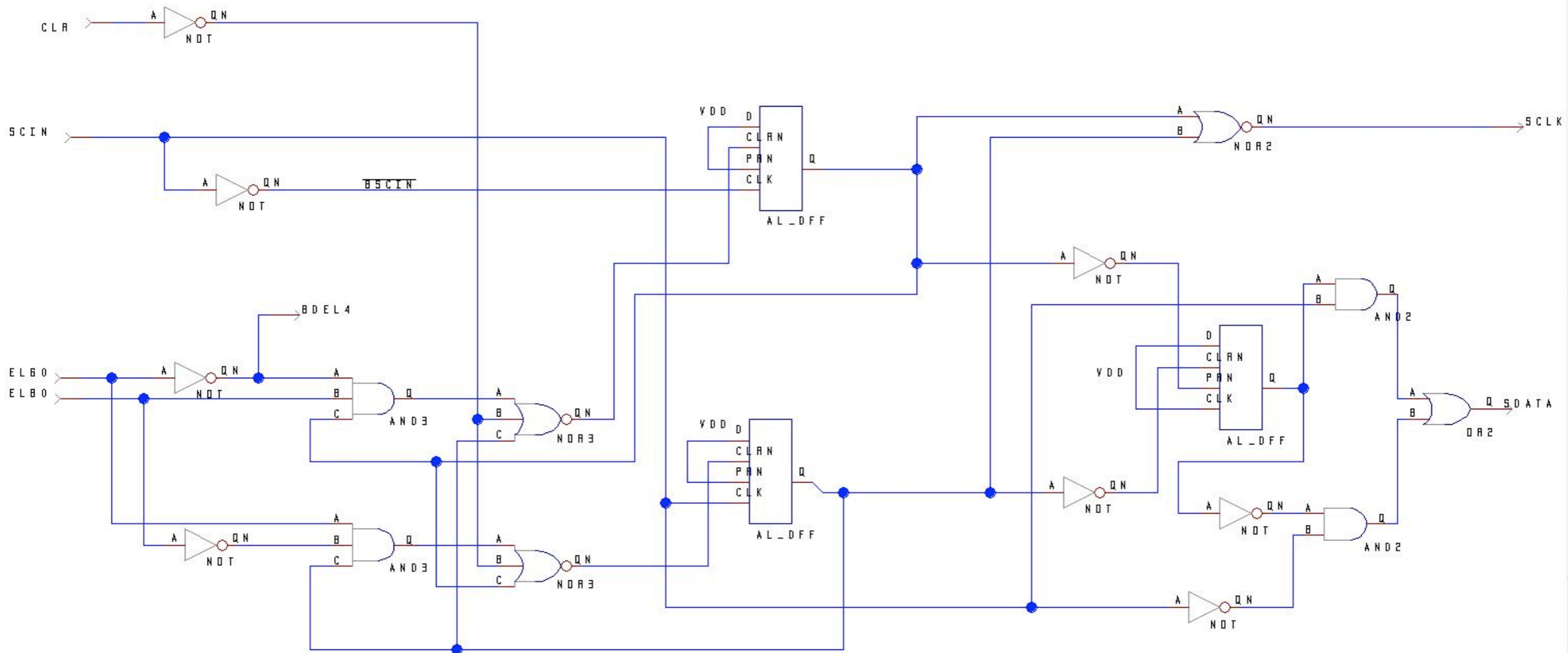
- output a pulse, of specified delay and width
- trigger a software action (process an EPICS record)

Each event receiver can be programmed to respond in a different way to the same event code.

# Event Timeline



# Example receiver



For  $\ll 1\%$  utilization of modern FPGA, get events within signal processing system.

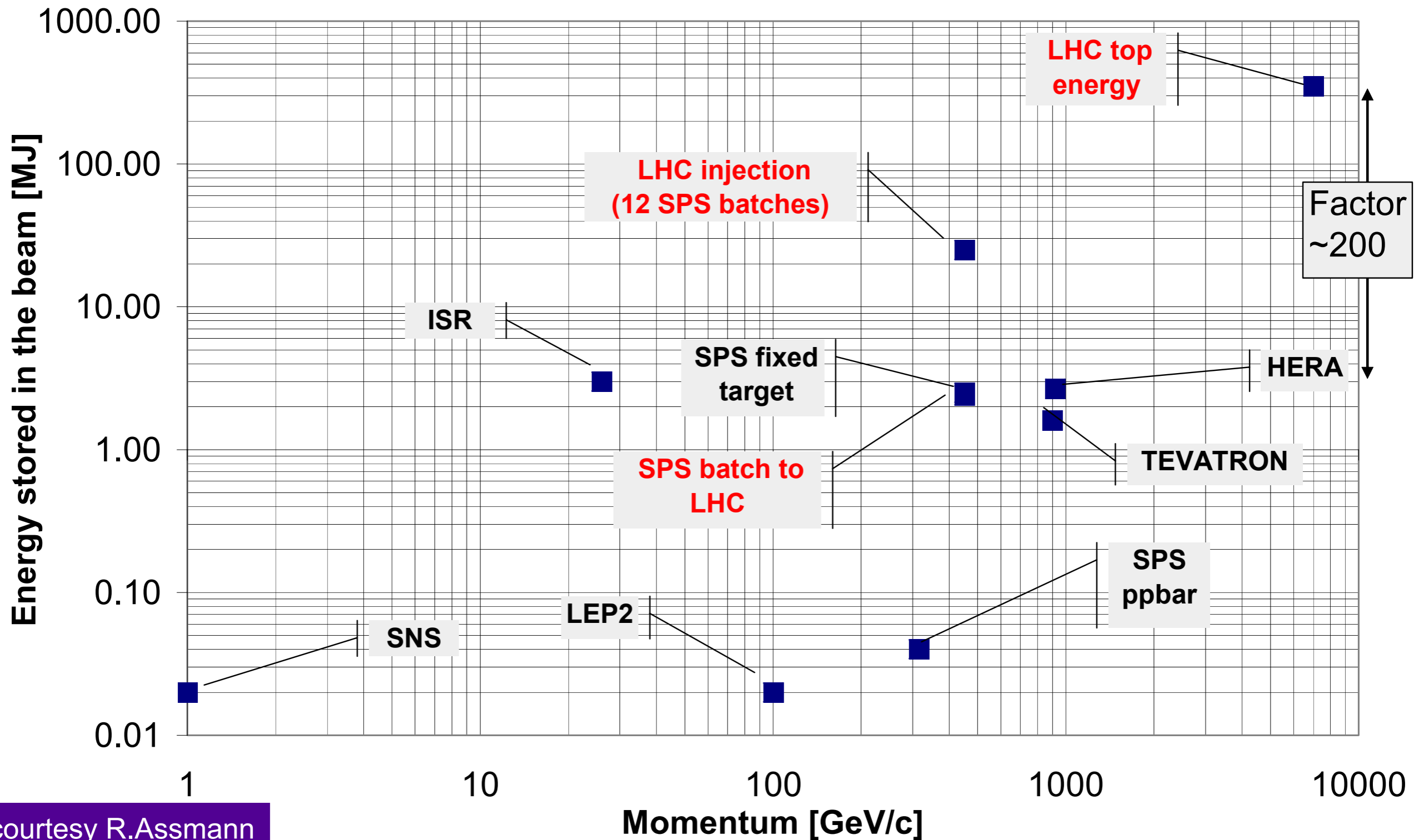
This example is in-house standard. Trend is to adopt standard PHY.

# Multimode Operation

- AKA: Multimode, Multiuser, Pulse to Pulse Modulation, Flavors, ...
- Different Beam Parameters
- Different feedforward tables
- Different results updated

# Machine Protection

# Motivation

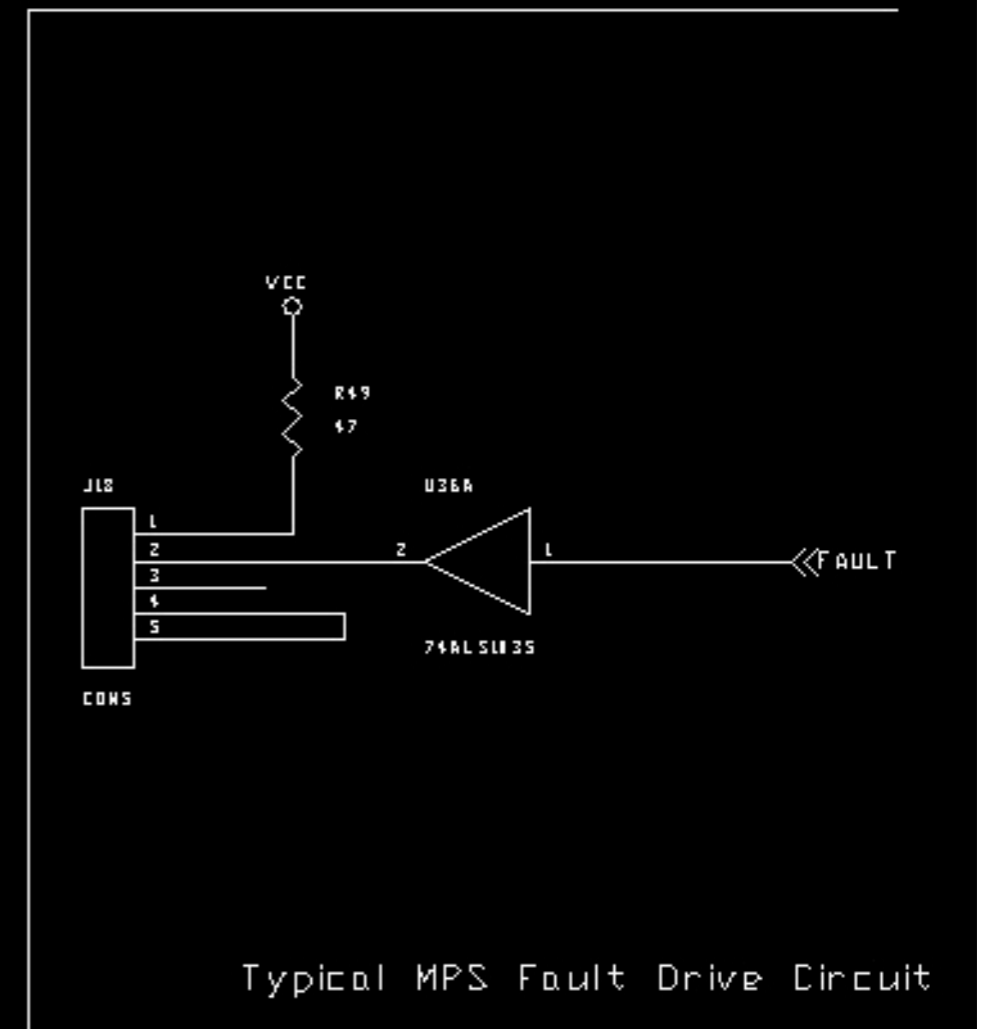
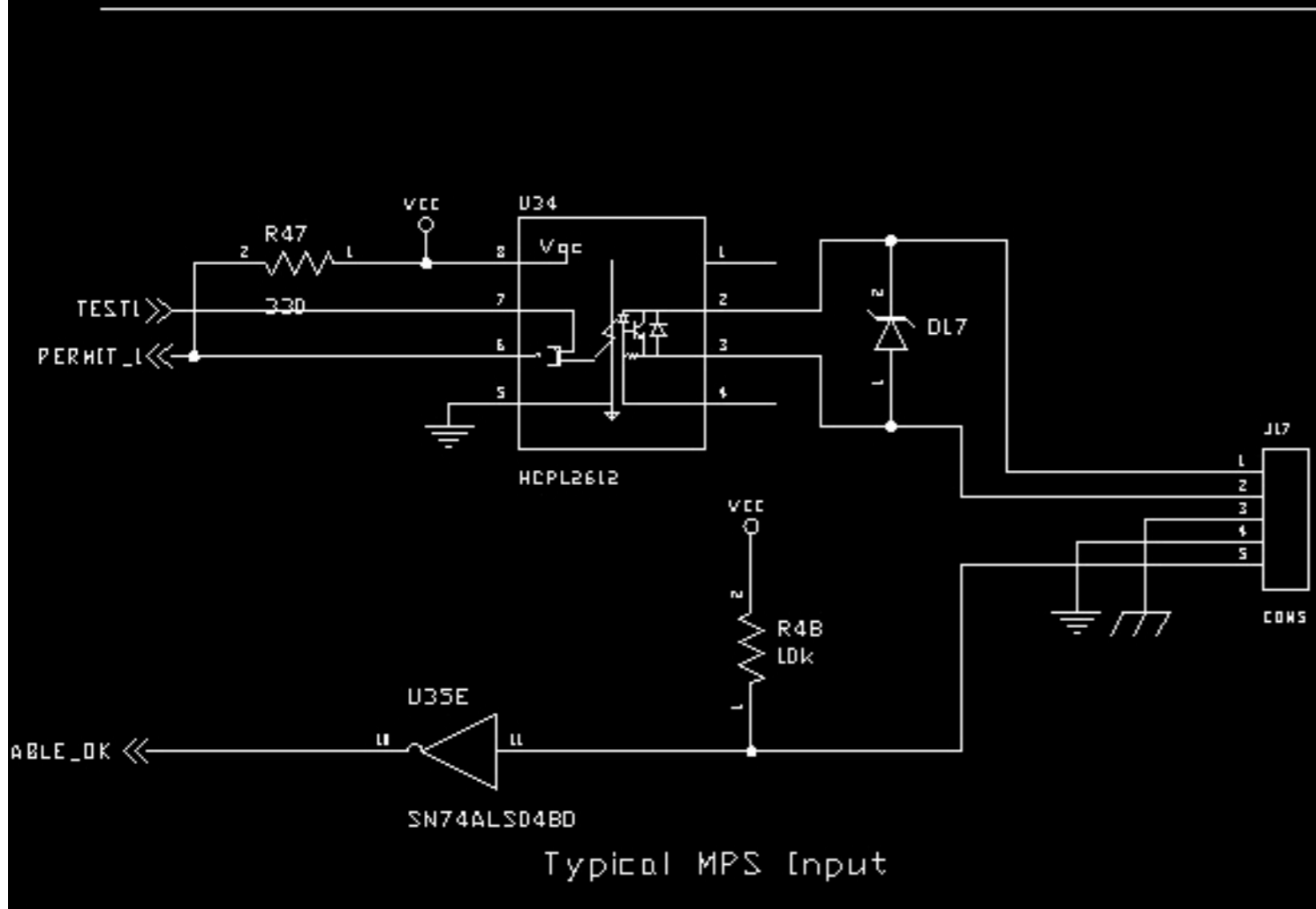




# Issues

- Subsystem drives MPS input
  - DSP detects loss of control
  - Differential current measurement detects beam loss
- Subsystem responds to MPS trip
  - Communicated on timing or real-time data broadcast system
  - Circular buffers

# Interface to MPS

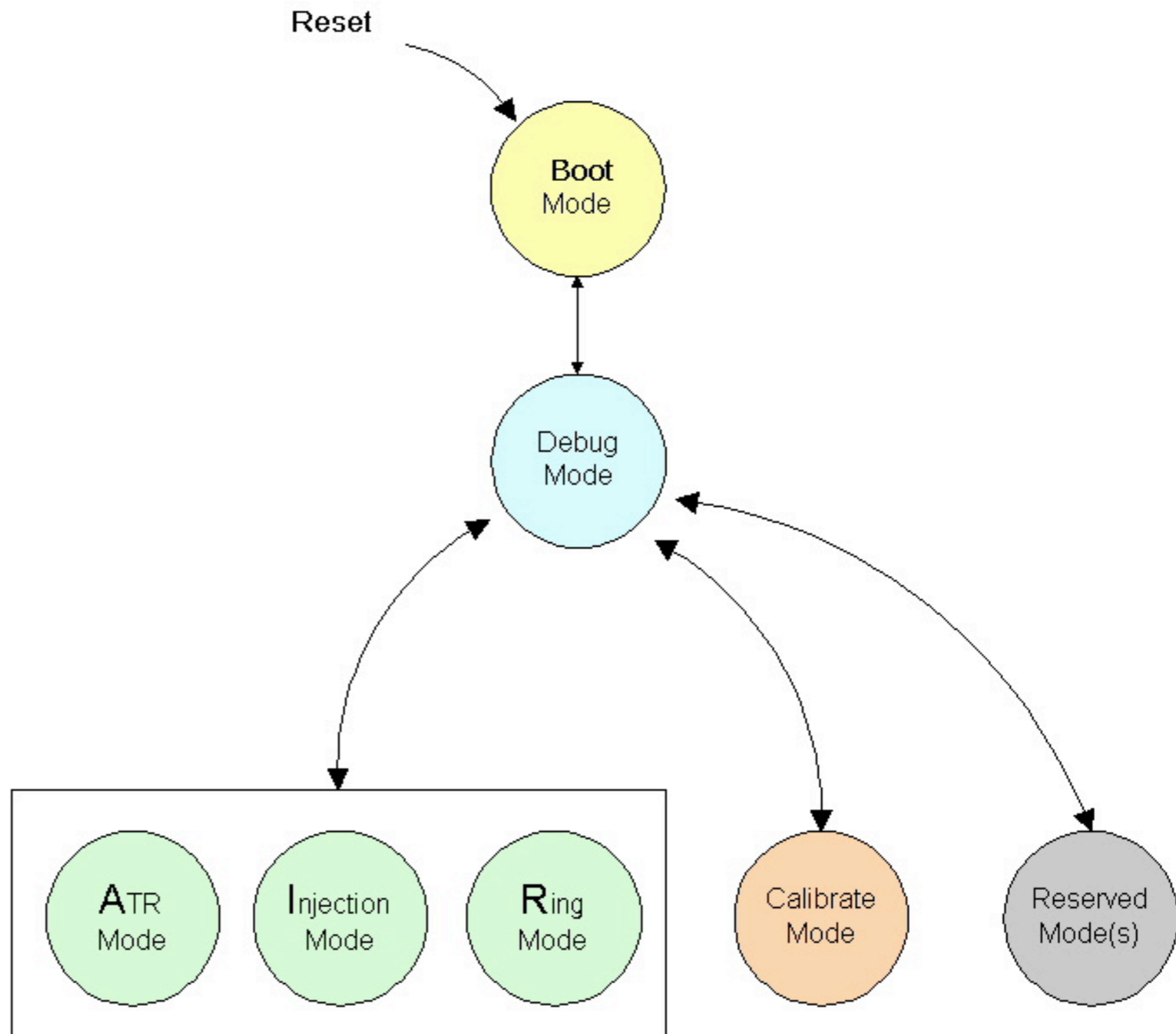


# Utility

- Temperature monitor
  - for fault monitoring (filter change time)
  - for correction of thermal effects
- Fan Speed
- Power supply current and voltage
- Heartbeat
  - monitored
  - optional watchdog timer for automatic reset
- Remote Power and Reset
  - Personnel access restrictions
  - Facility Size
    - MTTR

# Safe Reconfiguration

- avoiding the “turn antenna away from earth” command.
- protected boot memory containing communication code
- permanent communication subsystem (tiny IOC on a card, hard core on FPGA,...)
- Out of band communication as an option - but may add interconnect or cable in some cases

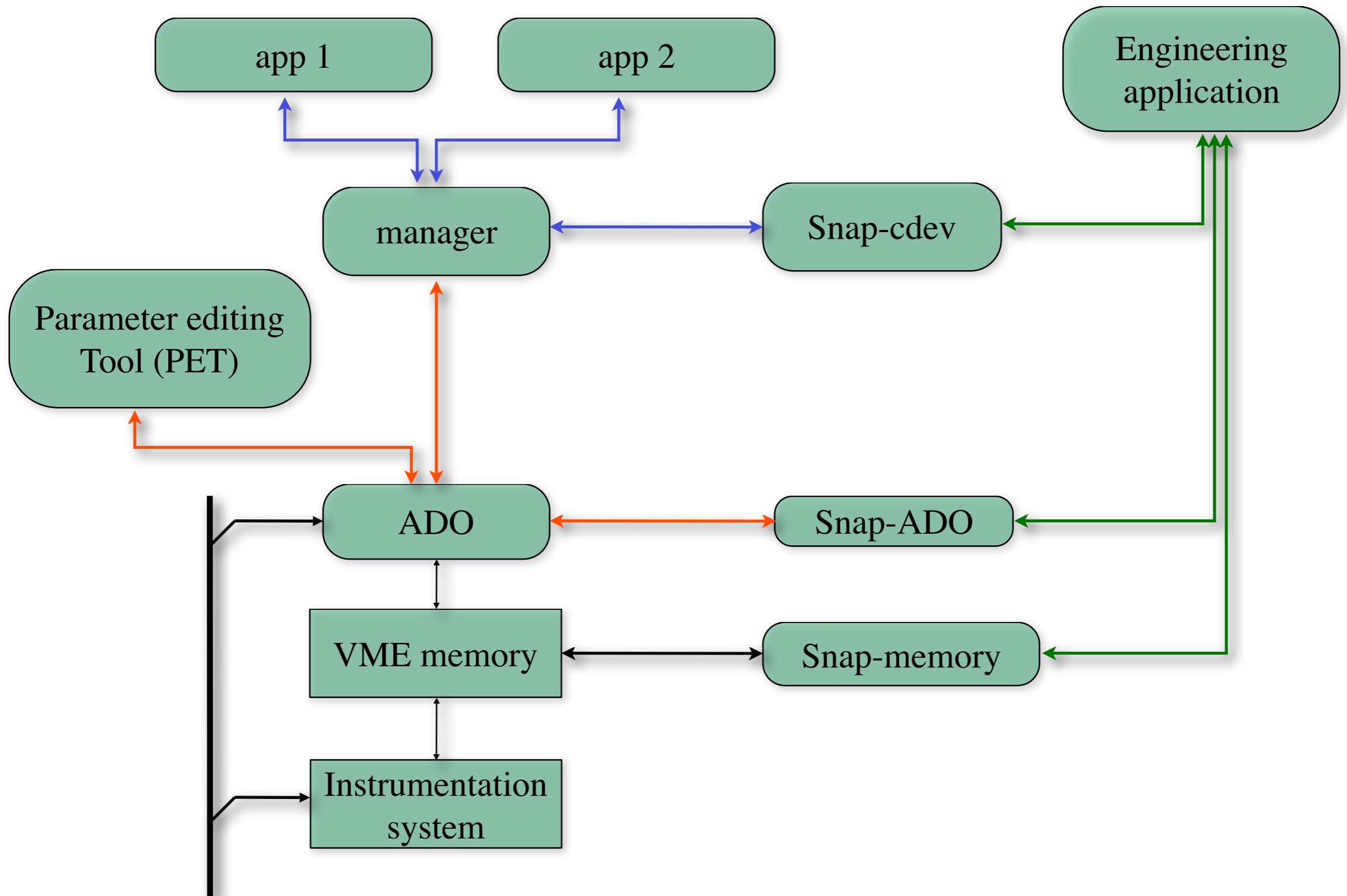


# Remote Debugging

by example

- RHIC BPM: Overview
  - Most electronics in radiation area
- SNS LLRF: In depth
  - SNS Equipment gallery put under access restrictions during commissioning

# RHIC Debugging Tools



Event links and RTDL



# Interface to LLRF Module

- Register based
  - Random read and write access to ease debugging
    - No "don't write during ..." conditions that require tricky timing.
    - No write-only registers that one cannot verify.
- Message based interfaces were avoided
  - Because they are harder to debug.
  - Also harder to implement in an FPGA, requiring parser.
  - One can easily trigger VME/VXI/PCI backplane analyzer on register access. Messages are harder.

# Register Documentation

## Register `LLRF_DDS_FREQ`

The offset frequency for the on-board Direct Digital Synthesizer (DDS). This is a signed 16-bit number that adjusts the frequency of cavity operation, relative to the Master Oscillator, in the range of  $\pm 625$  kHz. One bit corresponds to 19.073486328125 Hz exactly (assuming the RF sampling clock is a perfect 40 MHz).

## Register `LLRF_STATUS`

Read-only bit map of module status.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	-	-	-	CLP	FLT	LRC2	LRC1	PLL	IL	RF_ON	KCM

**CLP:** Latched indicator of occurrence of any premature termination of RF due to output magnitude clipping fault. Cleared at beginning of each pulse.

**FLT:** Latched indicator of occurrence of any premature termination of RF due to faults within the pulse. Cleared at beginning of each pulse.

**LRC2,LRC1:** FCM-specific readout of the configuration switches that define its position. 0=Left, 1=Center, 2=Right, 3=Invalid. Non-FCM systems read 0.

**PLL:** Instantaneous readout of the same signal described in the PLL bit of the

# "Single Source"

- Perl scripts convert Verilog register definitions into C++ include file, EPICS Database config, ...

```
register-map
SET_I      14'b000000000100000
SET_Q      14'b000000000100001
DDS_FREQ   14'b000000000100010
CONFIG     14'b000000000100011

llrf_defines.h
/* automatically generated by intercon.pl ../source/register
#define LLRF_CONFIG_ROM      (0x0000)
#define LLRF_ERRORS          (0x0010)
#define LLRF_STATUS          (0x0011)
#define LLRF_UCAPE           (0x0012)
#define LLRF_DCAPE           (0x0013)
#define LLRF_FCAPE           (0x0014)
#define LLRF_INT_STATUS      (0x0015)
#define LLRF_TTLTRG_MON      (0x0016)
#define LLRF_PEAK_ERR        (0x0017)
#define LLRF_PEAK_OUT        (0x0018)
#define LLRF_TOTALIZER       (0x001c)
#define LLRF_SHADOW          (0x0020)
#define LLRF_SET_I           (0x0020)
#define LLRF_SET_Q           (0x0021)
#define LLRF_DDS_FREQ        (0x0022)
#define LLRF_CONFIG          (0x0023)
```

# Debugging Registers: Console

- Via serial line or "telnet"

```
test-oper@rftf-test-opi-cow4:~
test-llrf-ioc-vxi> vxiHelp
VXI device support, version 2004-09-23 w/ write checks.

VXI helper routines:

NOTE: Test mode. A24 access actually
uses local RAM when the variable use_A24_TEST is set to 1.
Right now, use_A24_TEST is set to 0

    vxiHelp
    vxiInfo(int la)                - check given LA
    vxiRegister(const char *name, int la) - register LA (for dbior)
    vxiReport(int level)          - report on registered LAs
    vxiSearch()                   - Tests all LAs
    Word *vxiBoardAddr(int la)    - Get A16 base as seen by CPU
    void *vxiTestA24(int la)      - Check read access to A24 mem
    Bool vxiPeek(int la, int reg)  - Read A16 register
    Bool vxiPoke(int la, int reg, Word value) - Write A16 register
    void vxiMapA24(int la, unsigned long start) - Assign & enable A24 base addr.
    Word *vxiA24Addr(int la)     - Get A24 base as seen by CPU
    Bool vxiPeekA24(int la, int word) - Read A24 register
    Bool vxiPokeA24(int la, int word, Word value) - Write A24 register
    worddump(Word *addr, int count) - Dump memory by using 16-bit access
value = 83 = 0x53 = 'S'
test-llrf-ioc-vxi>
test-llrf-ioc-vxi> vxiPeekA24(0xD4, 0x22)
LA 0xD4, A24 word 0x22 = 0x0000
value = 1 = 0x1
test-llrf-ioc-vxi> █
```

# Debugging Registers:

- **Note:** Our hardware returns value **0xBAD** for undecoded registers (pullups & downs on data lines in case FPGA doesn't drive them)

VXI Registers, SCL\_LLRF:IOC01a

**A16 Read:**

LA (hex)	Register(hex, dec)	Value (hex)	(ASCII)	(Bits)
0xd4	0 0	0x4fa0	O_	
0xd4	0x1 1	0x1f4d	_M	

**A16 Write:**

LA (hex)	Register(hex, dec)	Value (hex)	Readback	(Bits)
0xd4	0 0	0	0x4fa0	
0	0 0	0	0xbad	

**A24 Read:**

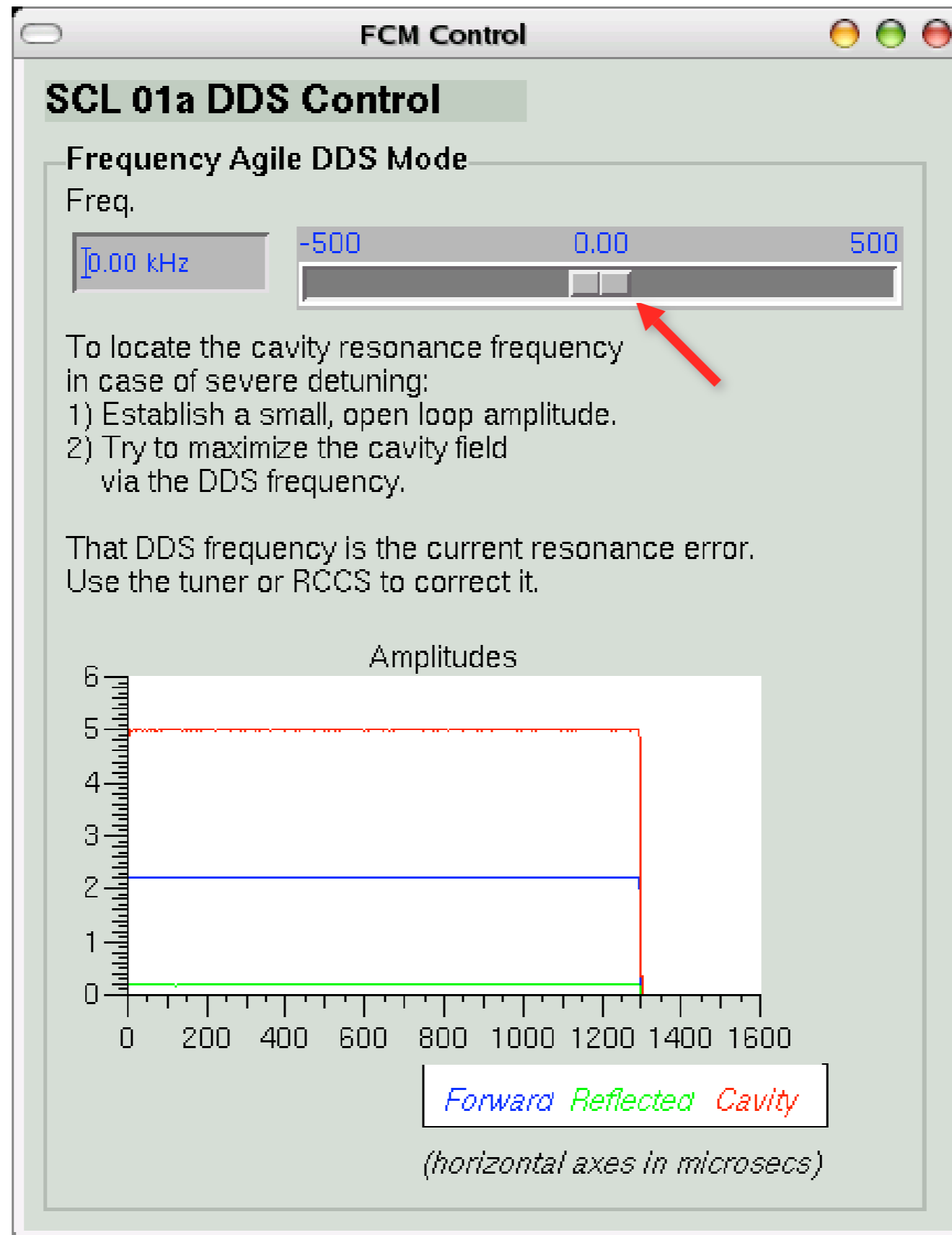
LA (hex)	Register(hex, dec)	Value (hex)
0xd4	0x22 34	0

**A24 Write:**

LA (hex)	Register(hex, dec)	Value (hex)
0xd4	0x22 34	0

Use WORD offsets (2-byte) f. Registers, press Return to send.

# End-User Register Access





# Other Debug Tools

- EPICS Sequencer and Database
  - Online, remote access to internal state
  - View the "raw" value behind some displayed data
  - Timestamps
  - Anything can be displayed on "Strip chart", or added to an archive tool for later analysis - good for infrequent events and unanticipated correlations
- Custom C/C++ Code
  - Access to internal data must be specifically added to the code
    - "Report" methods
    - Debug flags
    - Time stamps

# Source Code Control

# Version Control Benefits

- Serves as repository
  - Develop some bugfix on laptop, merge that into copy on the main development machine
  - Deploy "latest" version onto linac server
- "Roll back to state of January 18, 2006"
- View history of changes, compare different versions
  - "When did we add this behavior?"
  - "How was this handled 2 years ago?"

# CVS - Concurrent

- A free, open source version control system
  - Available for every operating system
  - Stable
  - Command-line, Emacs, Eclipse, ...
- **Handles text very well**
  - Plain ASCII or LaTeX documents
  - EPICS Sequencer and Database sources
  - C/C++
  - Verilog/VHDL
  - Front-end computer startup files
- For binary files, only date & comments available, no comparisons possible
  - Images, FPGA bitfiles, LabVIEW, ...
- Old
  - "subversion" might be better at handling directories

# CVS under Eclipse: Verilog

The screenshot displays the Eclipse IDE interface for comparing two versions of a Verilog file, `fdbk_loop.v`. The main window is titled "Compare fdbk\_loop.v 1.12 and 1.11".

**Left Panel (Navigator):** Shows a project tree with various Verilog files. The file `fdbk_loop.v 1.12` is selected.

**Center Panel (Text Compare):** Displays a side-by-side comparison of the Verilog code. The left pane shows the code for repository file `fdbk_loop.v 1.12`, and the right pane shows the code for `fdbk_loop.v 1.11`. The code includes assignments for wires like `e4_ls5`, `e4_int`, and `fdbk_err_wide`, and module instantiations like `trip` and `clip`. A blue highlight in the 1.12 version shows the addition of a `clip` module and an `assign` statement for `peak_out`.

**Bottom Panel (CVS History):** Shows the revision history for `fdbk_loop.v`. The table below summarizes the visible entries:

Revision	Tags	Revision Time	Comment
<b>Previous</b>			
*1.12		2/14/07 12:13 PM	firmware with output clipping
1.11		1/12/06 3:42 PM	get new firmware

# FPGA Firmware Handling

- Verilog sources are in CVS
  - Full benefit of version comparisons
- Bitfiles also in CVS as 'binary'
  - No insight into changes, but since each "place-and-route" creates different bitfile, it's good to keep a copy of the specific bitfile
- Front-end computer programs FPGA
  - Loads bitfile via network

*(For machine protection related FPGA, bitfile is in local EEPROM)*



# Configuration Control

# SNS Device Database

Active configuration file stored here.  
Supported by rest of purple tables which include historic.

Diagnostics IOC Active Configuration		
IOC Config Type Id (FK)	VARCHAR(25)	NOT NULL
Maj Ver Nbr (FK)	NUMERIC(3,0)	NULL
Min Ver Nbr (FK)	NUMERIC(4,0)	NULL
Cmnt	VARCHAR(2000)	NULL
Modify Date	DATE	NOT NULL
Mod By Bn	VARCHAR(6)	NOT NULL

Diagnostics IOC Configuration History		
IOC Config Type Id (FK)	VARCHAR(25)	NOT NULL
Maj Ver Nbr (FK)	NUMERIC(3,0)	NOT NULL
Min Ver Nbr (FK)	NUMERIC(4,0)	NOT NULL
Cmnt	VARCHAR(2000)	NULL
Modify Date	DATE	NOT NULL
Mod By Bn	VARCHAR(6)	NOT NULL

Diagnostics IOC Parameter Group		
IOC Config Type Id (FK)	VARCHAR(25)	NOT NULL
Maj Ver Nbr (FK)	NUMERIC(3,0)	NOT NULL
Grp Cnt	NUMERIC(3,0)	NOT NULL
Prmr Grp Nm	VARCHAR(25)	NULL
Cmnt	VARCHAR(2000)	NULL

Diag IOC Config Maj Ver		
IOC Config Type Id (FK)	VARCHAR(25)	NOT NULL
Maj Ver Nbr	NUMERIC(3,0)	NOT NULL
Cmnt	VARCHAR(2000)	NULL
Modify Date	DATE	NOT NULL
Mod By Bn	VARCHAR(6)	NOT NULL

Diagnostics IOC Parameter		
IOC Config Type Id (FK)	VARCHAR(25)	NOT NULL
Maj Ver Nbr (FK)	NUMERIC(3,0)	NOT NULL
Grp Cnt (FK)	NUMERIC(3,0)	NOT NULL
Prmr Cnt	NUMERIC(4,0)	NOT NULL
Prmr Nm	VARCHAR(50)	NOT NULL
Prmr Type Id (FK)	VARCHAR(25)	NOT NULL

Parameter Datatype		
Prmr Type Id	VARCHAR(25)	NOT NULL
Datatype Precs	NUMERIC(3,0)	NULL

Diagnostics IOC Parameter Value

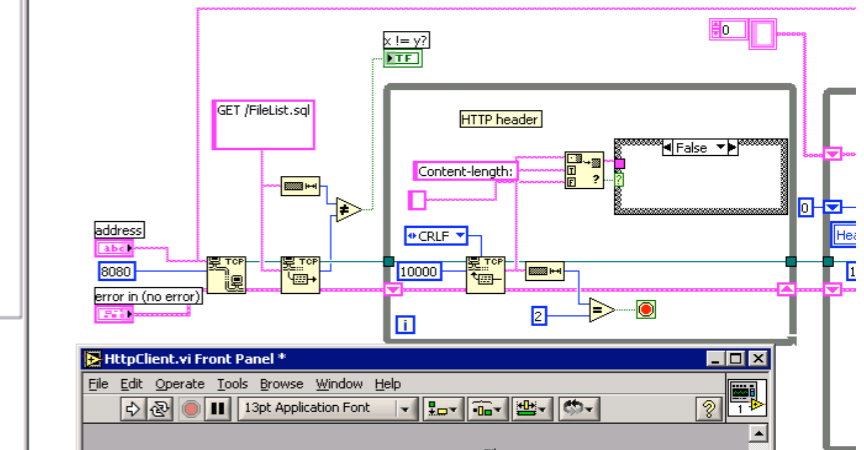
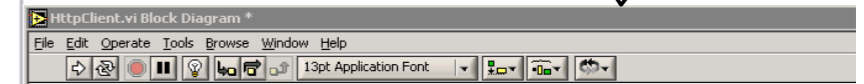
Device		
Dvc Id	VARCHAR(40)	NOT NULL
Dvs Id (FK)	VARCHAR(10)	NULL
Subtype Id (FK)	VARCHAR(10)	NULL
Dvc Type Id (FK)	VARCHAR(25)	NULL
Dvc Inst	VARCHAR(25)	NULL
Parent Dvc Id (FK)	VARCHAR(40)	NULL
Dvc Desc	VARCHAR(255)	NULL
BL Dvc Ind	CHAR(1)	NOT NULL
Virtual Dvc Ind	CHAR(1)	NOT NULL
Invalid Id Ind	CHAR(1)	NOT NULL
Dvc Id Alias	VARCHAR(75)	NULL
Act Dvc Ind	CHAR(1)	NOT NULL
MPS Dvc Ind	CHAR(1)	NOT NULL
Dvc Dns Nbr	VARCHAR(50)	NULL
Dns Dvc Id	VARCHAR(40)	NULL
Mod By Uid	VARCHAR(64)	NULL
Mod Dte	DATE	NULL
Owner Cat Id	VARCHAR(10)	NULL

IOC Configuration File		
Dvc Id (FK)	VARCHAR(40)	NOT NULL
Config File Nm	VARCHAR(255)	NOT NULL
Config File Loc	VARCHAR(128)	NULL
Config File Nbr	NUMERIC(50,0)	NULL
Contents	LONG VARCHAR	NULL
Modify Date	DATE	NOT NULL
Mod By Uid	VARCHAR(64)	NOT NULL
Editable Indicator	CHAR(1)	NOT NULL

IOC Config File Hist		
Dvc Id (FK)	VARCHAR(40)	NOT NULL
Config File Nm	VARCHAR(100)	NULL
Modify Date	DATE	NOT NULL
Config File Loc	VARCHAR(128)	NULL
Config File Cont	TEXT	NULL
Mod By Uid	VARCHAR(64)	NOT NULL

Input Output Controller Device		
Dvc Id (FK)	VARCHAR(40)	NOT NULL
IP Addr	VARCHAR(50)	NULL
Ether Addr	VARCHAR(50)	NULL
Net Domain	VARCHAR(50)	NULL
Net Mask	VARCHAR(50)	NULL
IOC Net Nm	VARCHAR(50)	NULL
VLAN Nbr	VARCHAR(30)	NULL
Sw Dvc Id (FK)	VARCHAR(40)	NULL
Sw Port Nbr	NUMERIC(2,0)	NULL
TDrv Dvc Id (FK)	VARCHAR(40)	NULL
TDrv Port Nbr	VARCHAR(50)	NULL
RPC Dvc Id (FK)	VARCHAR(40)	NULL
RPC Addr	VARCHAR(30)	NULL
IOC Ser Nbr	VARCHAR(50)	NULL
Tty Nm	VARCHAR(50)	NULL
VxWorks Nbr	VARCHAR(50)	NULL
OPU Type	VARCHAR(50)	NULL
Boot Params	VARCHAR(50)	NULL
EPICS Version	VARCHAR(50)	NULL
Status	VARCHAR(50)	NULL
Reset Id	NUMERIC(12,6)	NULL
Dsgn Cab Slot Bgn	NUMERIC(3,0)	NULL
Dsgn Cab Slot End	NUMERIC(3,0)	NULL
Dsgn Cab Slot Pos Ind	CHAR(1)	NOT NULL
Pos Within Slots	NUMERIC(3,0)	NULL
Boot Dte	DATE	NULL
Boot Grv	VARCHAR(128)	NULL
Boot File	VARCHAR(255)	NULL
VxWorks BDP Ver	VARCHAR(25)	NULL
VxStat Ver	VARCHAR(50)	NULL
Gateway Adr	VARCHAR(50)	NULL
Login Nm	VARCHAR(64)	NULL
Parse Ind	CHAR(1)	NOT NULL
IOC Config Type Id (FK)	VARCHAR(25)	NOT NULL

Files pulled from here.



IOC Application which pulls Configuration file to IOC from RDB. Uses HTTP Socket Library TCP/IP to connect to Web server Web Server uses standard RDB connectivity: PHP, JSP, ASP

```

BEGIN
  SELECT config_file_nm, config_file_loc
  INTO v_config_file_nm, v_config_file_loc
  FROM epics.ioc_config_type
  WHERE ioc_config_type_id = (SELECT ioc_config_type_id
                              FROM epics.ioc_dvc
                              WHERE dvc_id = p_dvc_id);

EXCEPTION
  WHEN NO_DATA_FOUND
  THEN
    RAISE;
END;

SELECT maj_ver_nbr, min_ver_nbr, ioc_config_type_id
INTO v_maj_ver_nbr, v_min_ver_nbr, v_ioc_config_t
FROM diag_ioc_act_config
WHERE dvc_id = p_dvc_id;
EXCEPTION
  WHEN NO_DATA_FOUND
  THEN
    ops$oracle.global_utils.v_errornum := SOLCODE;
    
```

Portion of stored procedure used when IOC Configuration File generation UI creates a new configuration file for a given IOC. These selects confirm active versions which then dictate data to be used to create the file stored for use.

# Example: LLRF Multiplicity

- Almost 100 SNS LLRF Systems, handled by ~50 front-ends
  - As different as warm vs. super-conducting cavities
- One source base for all of them
  - Differences handled by configuration settings
  - If possible, startup files and overview displays script-generated from central system info.

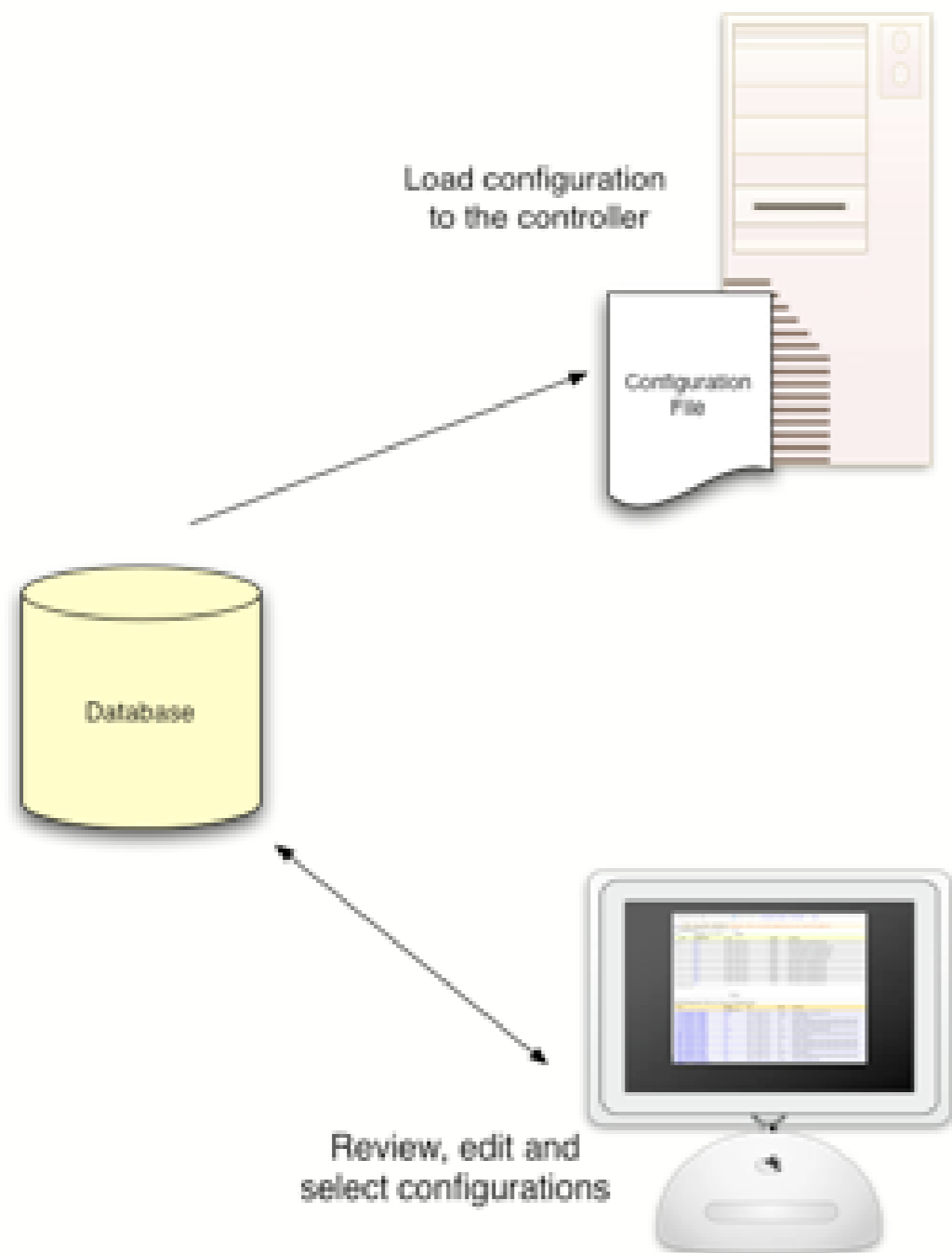
NC Linac				Medium beta SCL				High beta SCL							
	RF	MPS	Loop/AFF		RF	MPS	Loop/AFF		RF	MPS	Loop/AFF		RF	MPS	Loop/AFF
RFQ 1 (0)	■	■	■ On	01a (15)	■	■	■ On	06c (32)	■	■	■ On	12a (48)	■	■	■ On
MEBT 1 (1)	■	■	■ On	01b (16)	■	■	■ On	07a (33)	■	■	■ On	12b (49)	■	■	■ On
MEBT 2 (2)	■	■	■ On	01c (17)	■	■	■ On	07b (34)	■	■	■ On	12c (50)	■	■	■ On
MEBT 3 (3)	■	■	■ On	02a (18)	■ disabled	■	■ On	07c (35)	■	■	■ On	12d (51)	■ disabled	■	■ On
MEBT 4 (4)	■	■	■ On	02b (19)	■	■	■ On	08a (36)	■	■	■ On	13a (52)	■	■	■ On
DTL 1 (5)	■	■	■ On	02c (20)	■	■	■ On	08b (37)	■	■	■ On	13b (53)	■	■	■ On
DTL 2 (6)	■	■	■ On	03a (21)	■	■	■ On	08c (38)	■	■	■ On	13c (54)	■	■	■ On
DTL 3 (7)	■	■	■ On	03b (22)	■	■	■ On	09a (39)	■	■	■ On	13d (55)	■	■	■ On
DTL 4 (8)	■	■	■ On	03c (23)	■	■	■ On	09b (40)	■ disabled	■	■ On	14a (56)	■	■	■ On
DTL 5 (9)	■	■	■ On	04a (24)	■	■	■ On	09c (41)	■	■	■ On	14b (57)	■	■	■ On
DTL 6 (10)	■	■	■ On	04b (25)	■	■	■ On	10a (42)	■	■	■ On	14c (58)	■ disabled	■	■ On
CCL 1 (11)	■	■	■ On	04c (26)	■	■	■ On	10b (43)	■	■	■ On	14d (59)	■	■	■ On
CCL 2 (12)	■	■	■ On	05a (27)	■	■	■ On	10c (44)	■	■	■ On	15a (60)	■	■	■ On
CCL 3 (13)	■	■	■ On	05b (28)	■	■	■ On	11a (45)	■	■	■ On	15b (61)	■	■	■ On
CCL 4 (14)	■	■	■ On	05c (29)	■	■	■ On	11b (46)	■ disabled	■	■ On	15c (62)	■	■	■ On
				06a (30)	■	■	■ On	11c (47)	■	■	■ On	15d (63)	■	■	■ On
				06b (31)	■	■	■ On					16a (64)	■	■	■ On

**Legend:**  
AI RF Ampl. off Auto-Run goal  
PI RF Phase is shifted

# Configuration File Strategy

- Track changes to configuration files
  - Who made the change
  - When was the change made
  - Why was the change made
- Restore past configuration files when necessary
- Configuration consists of **structure** and **data**
  - Structure (collection of properties that describe the device) is typically common across devices of a specific type
  - Data typically varies for each device and represents the values for a device's properties
  - Structure is associated with a configuration's major version number and data is associated with the minor version

# Configuration File Storage/Retrieval



Configuration Type:  Device Overview | [Configuration Templates](#) | [Batch Import](#) | [Logout](#)

[Close](#) DTL\_Diag:IOC\_BCM622 *Warning: This is not the default device for your IP Address!*

25 Configurations Display  items Page  of 3

no file selected

Active	Configuration	Date	Author	Comment
<input checked="" type="radio"/>	<a href="#">17.22</a>	May 01, 2007 16:14	900688	Batch upload of configuration files.
<input type="radio"/>	<a href="#">17.21</a>	May 01, 2007 15:48	900688	Demo Batch upload of configuration files.
<input type="radio"/>	<a href="#">17.20</a>	May 01, 2007 11:36	900688	Test batch upload of configuration files.
<input type="radio"/>	<a href="#">17.19</a>	May 01, 2007 11:36	900688	Test batch upload of configuration files.
<input type="radio"/>	<a href="#">17.18</a>	May 01, 2007 10:46	900688	Batch upload of configuration files.
<input type="radio"/>	<a href="#">17.17</a>	May 01, 2007 10:44	900688	Batch upload of configuration files.
<input type="radio"/>	<a href="#">17.16</a>	May 01, 2007 10:43	900688	Batch upload of configuration files.
<input type="radio"/>	<a href="#">17.15</a>	May 01, 2007 10:42	900688	Batch upload of configuration files.
<input type="radio"/>	<a href="#">17.14</a>	May 01, 2007 10:41	900688	Batch upload of configuration files.
<input type="radio"/>	<a href="#">17.13</a>	May 01, 2007 10:40	900688	Batch upload of configuration files.

Activation notes:

BCM Diagnostic Device Active Configurations:

Device	Active Configuration	Date	Editor	Comment
<a href="#">CCL Diag:IOC_BCM102</a>	<a href="#">14.22</a>	May 01, 2007 16:14	900688	Batch upload of configuration files.
<a href="#">DTL Diag:IOC_BCM400</a>	<a href="#">11.1</a>	Nov 13, 2006 14:51	900688	Use the INI file.
<a href="#">DTL Diag:IOC_BCM428</a>	<a href="#">2.1</a>	May 31, 2006 14:28	9PJ	Original Configuration taken during initial insert May 2006
<a href="#">DTL Diag:IOC_BCM600</a>	<a href="#">2.1</a>	May 31, 2006 14:28	9PJ	Original Configuration taken during initial insert May 2006
<a href="#">DTL Diag:IOC_BCM622</a>	<a href="#">17.22</a>	May 01, 2007 16:14	900688	Batch upload of configuration files.
<a href="#">EDmp Diag:IOC_BCM02</a>	<a href="#">4.1</a>	May 31, 2006 14:28	9PJ	Original Configuration taken during initial insert May 2006
<a href="#">HEBT Diag:IOC_BCM01</a>	<a href="#">12.1</a>	Nov 13, 2006 14:52	900688	Use the INI file.
<a href="#">HEBT Diag:IOC_BCM09</a>	<a href="#">2.1</a>	May 31, 2006 14:28	9PJ	Original Configuration taken during initial insert May 2006
<a href="#">HEBT Diag:IOC_BCM20</a>	<a href="#">2.1</a>	May 31, 2006 14:28	9PJ	Original Configuration taken during initial insert May 2006
<a href="#">HEBT Diag:IOC_BCM32</a>	<a href="#">2.1</a>	May 31, 2006 14:28	9PJ	Original Configuration taken during initial insert May 2006
<a href="#">IDmp Diag:IOC_BCM01</a>	<a href="#">11.1</a>	Nov 16, 2006 12:55	900688	Use the INI file.
<a href="#">LDmp Diag:IOC_BCM05</a>	<a href="#">2.1</a>	May 31, 2006 14:28	9PJ	Original Configuration taken during initial insert May 2006
<a href="#">LEBT Diag:IOC_BCM1t4</a>	<a href="#">11.1</a>	May 01, 2007 11:44	900688	Test new activation code.

# Implementation Choices

Flexibility  
Rapid development



Performance

- Human
- Commercial/Scripted High Level
- High Level Application (Multiuser OS)
- Low Level Application (RTOS target)
- Embedded (DSP, limited OS)
- FPGA
- ASIC
- Analog

“Some folk built like this, some folk built like that  
But the way I'm built, you shouldn't call me fat  
Because I'm built for comfort, I ain't built for speed...”

- Willie Dixon

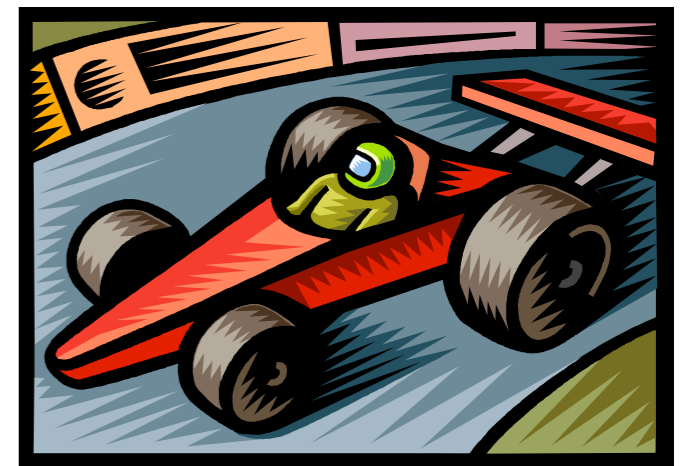
# Flexibility or Performance?

- Flexibility in the form of
  - Rapid development, independent testing, remote access, online changes, rich set of debug tools



... often differs from ...

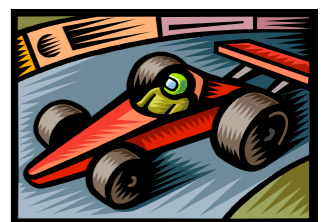
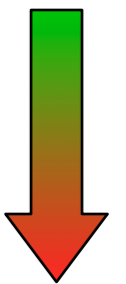
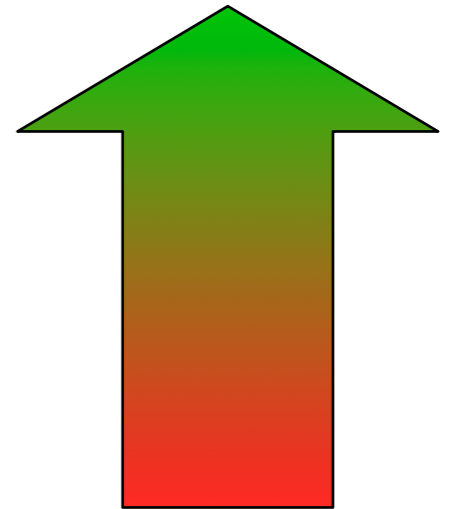
- Performance
  - Fast startup times, short response times, deterministic "real time" behavior.





# SNS LLRF Choices

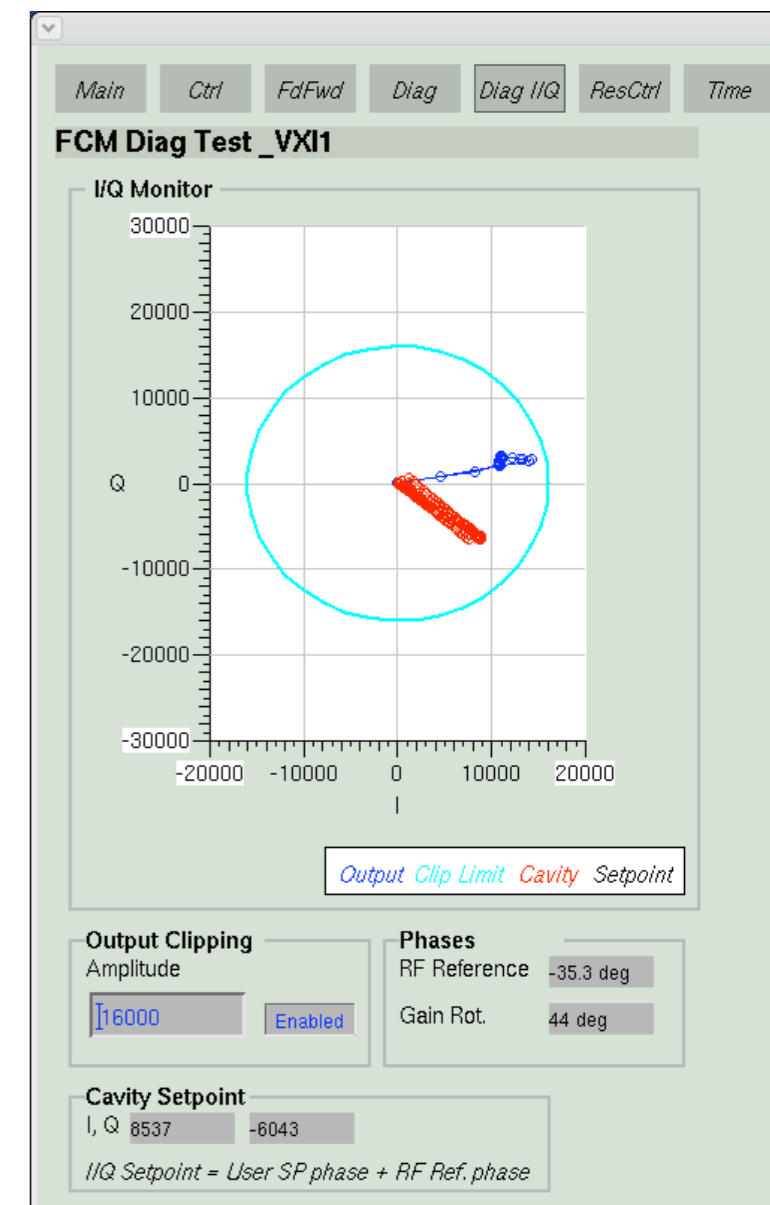
- Software based a control system **framework**  
(Experimental Physics and Industrial Control System, EPICS)
  - Matlab scripts for test & development of algorithms
  - Front-End computer uses EPICS **State Machine Tool** for automation, and "runtime **Database**" for data flow.
  - C/C++ driver code
- 
- **Fast** Feedback (~40MHz) and interlocks in **Verilog**, VHDL, AHDL. Several Iterations
  - Hardware as simple as possible: Analog filtering, ADCs/DACs, then **FPGA**





# Operator Interface: Display Manager

- Drawing package for
  - Placing labels, text-monitors, meters, ... on a screen
  - Connecting them to online Process Variables
  - Display panel **Configuration** instead of coding

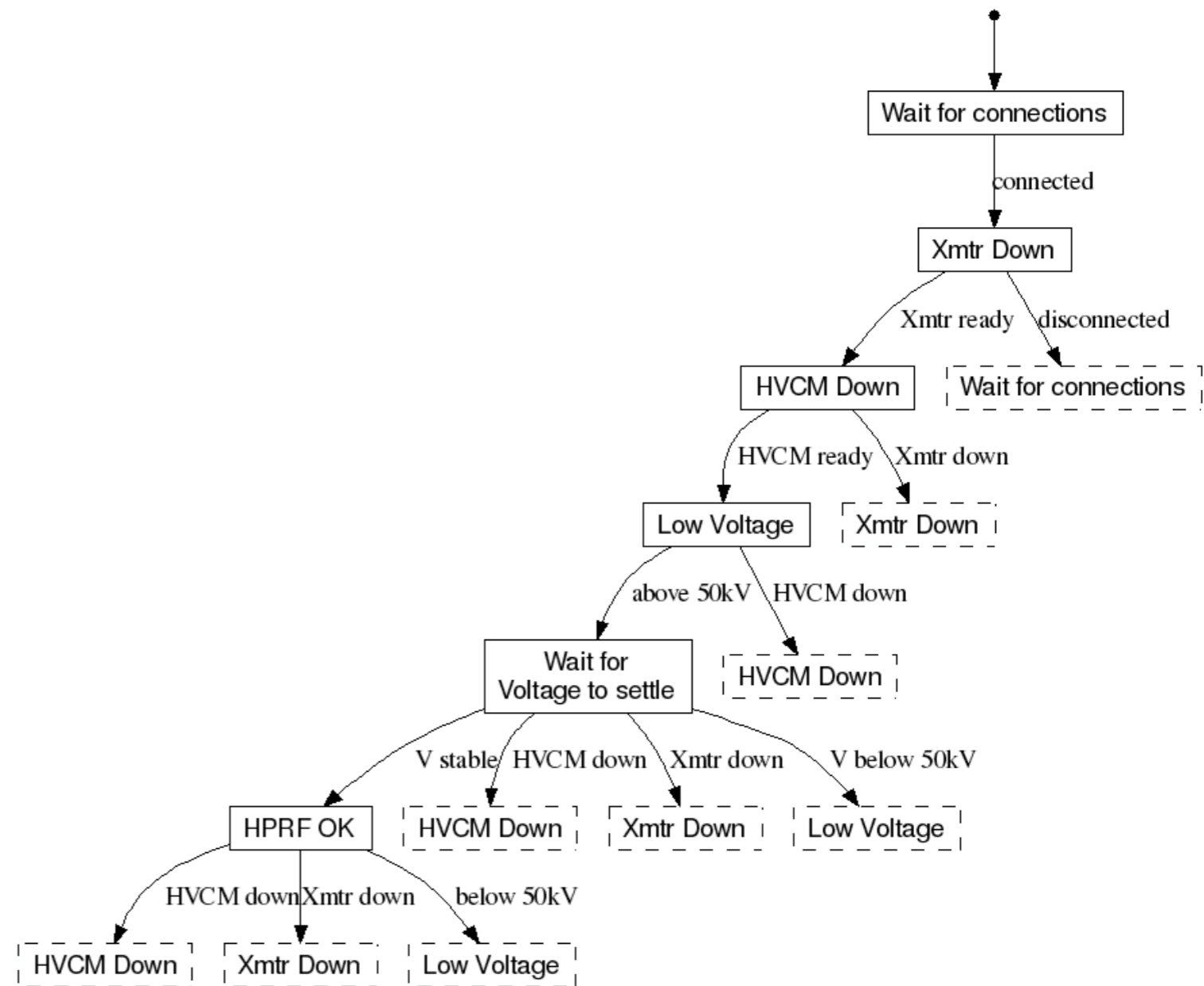


# Overall SNS LLRF

- Requirements change, so **Flexibility** is key.
- Resonance Error computation, feedback loop setup, ...
  - If possible, first developed in Matlab
  - Then implemented on Front-End as State Machine or EPICS Database
  - If necessary, later moved into custom C++ driver code, or even FPGA

# State Machine (EPICS "Sequencer")

- Used for automation whenever possible
- "On Demand" tasks, response times of .1 to 1 sec
- Safest and most flexible tool
  - Runs on host as well as front-end
  - Start/Stop/Update without front-end reboot



# EPICS "Database"

- Used for steady-state control, data flow.
- **Full remote access** to any detail.
- Limited online changes.
- "Records", building blocks
  - Read input, computation, write output, ...
- Database Engine handles
  - Periodic or event-driven scanning
  - Time stamps(!)
  - Check of alarm limits
  - Publication of data in "Process Variables"
- Response times of millisecs possible, or more than 10000 records per front-end computer.

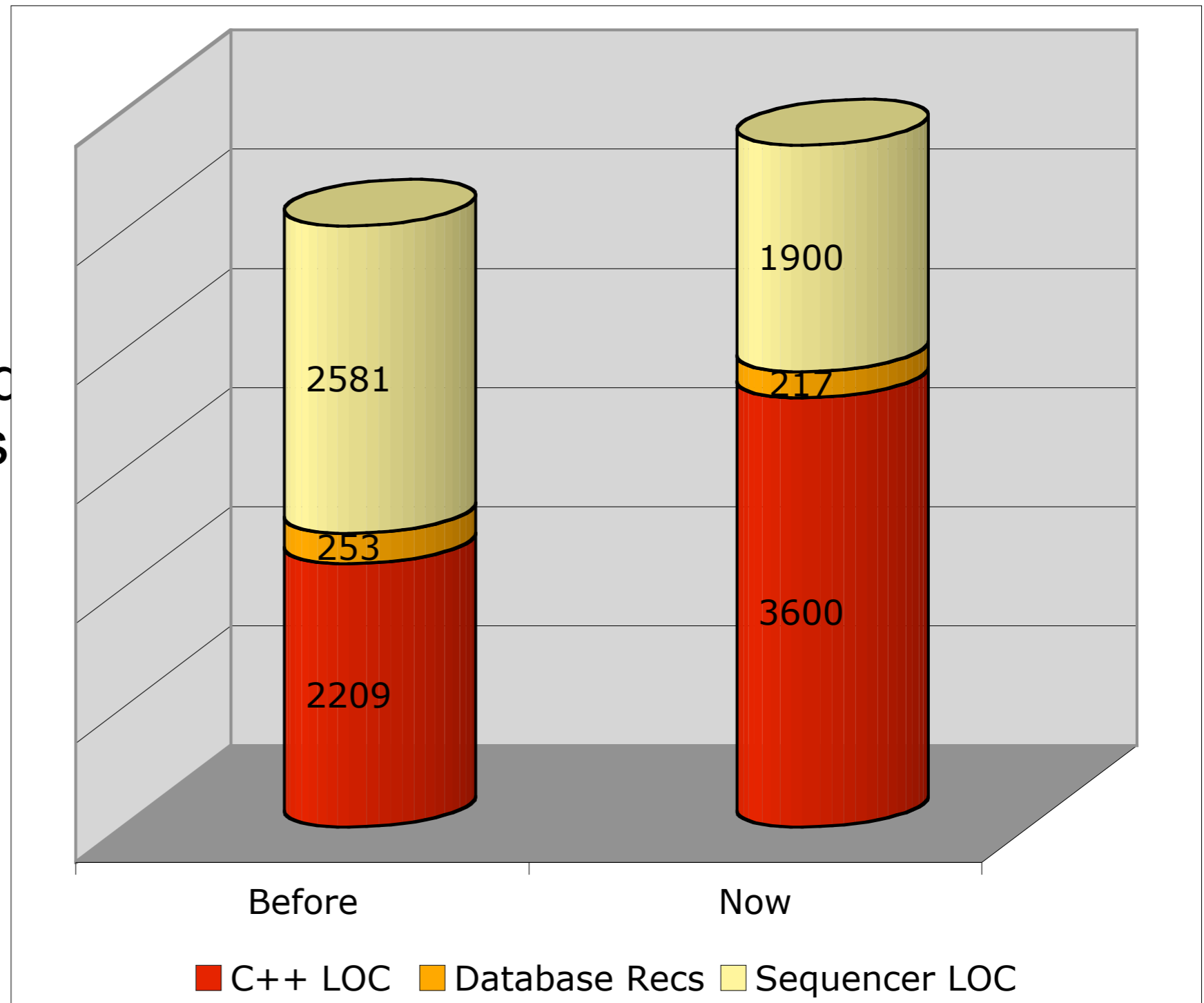
```
record(ai, "temp")
{
    SCAN "1 second"
    INP          "#C2"
    S3"
    EGU          "deg C"
    HIGH        "40.0"
    ...
}
```

# Custom Low Level Code

- Custom C/C++
  - When required for higher **performance**, or interrupt service routines, low-level access to custom hardware
  - Usually **no** online changes.
  - It's really **hard** to understand, extend, debug somebody else's custom code
  - Debug tools vary with operating system
    - SNS, using vxWorks5 with Linux hosts has currently no online source-level debugger....
- **FPGA**
  - Same **problems** as custom C/C++ code
    - Probably even more so, since HDL is a "code", but often not implemented by software engineers.
  - Good simulation and offline analysis tools but online debugging limited to scope, signal analyzer.

# SNS LLRF Changes in early 2007

- Improve performance of tested algorithms by converting Sequencer (State Machine) code and Database Records to C++



# Alternative DSP Implementations

- High level environment
  - Commercial
  - Physics application framework
- Within control system toolkit
- Vertically integrated commercial products

# Matlab Scripting

## Example

### Orbit correction

```
% Get the vertical orbit
Y = getam('BPMY');

% Get the Vertical response matrix from the model
Ry = getrespmat('BPMY', 'VCM');    % 120x70 matrix

% Computes the SVD of the response matrix
lvec = 1:48;
[U, S, V] = svd(Ry, 0);

% Find the corrector changes use 48 singular values
DeltaAmps = -V(:,lvec) * S(lvec,lvec)^-1 * U(:,lvec)' * Y;

% Changes the corrector strengths
stepsp('VCM', DeltaAmps);
```



# LabVIEW FPGA with EPICS

