1. Abstract

The Giga Bit Transceiver based Expandable Front-End (GEFE) is a multipurpose FPGA-based radiation tolerant card, produced under the CERN Open Hardware License (CERN OHL). It is foreseen to be the new standard FMC carrier for digital front-end applications in the CERN BE-BI group. Its intended use ranges from fast data acquisition systems to slow control installed close to the beamlines, in a radioactive environment exposed to total ionizing doses of up to 75 krad (750 Gy). This poster introduces the architecture of the GEFE, its features as well as examples of its application in different setups.

2. The GEFE

2.1 Radiation Tolerant

Target Total Ionizing Dose (TID): up to 75 krad

In order to maximize its radiation tolerance, the number of active components has been reduced as much as possible in terms of number and type. These components are either radiation tolerant by design (e.g. the GBTx, VTRx, etc.), capable to stand a TID in the order of Mdy or Components-On-The-Shelf (COTS) qualified for a TID up to 750 Gy, in GEFE, the critical COTS (all CMOS-based) are not affected by displacement damage and present very low SEE cross section. Moreover, the ProASIC3 FPGA (the main COTS of the GEFE board) features flash-based configuration memory, immune to SEE as well as mitigation techniques that may be implemented in the user logic. The maximum acceptable system SEE cross section is application dependent. The TID is the most critical radiation effect, since it determines whether the COTS will withstand the expected doses of radiation without permanent damage. The target TID level of the GEFE board has been set to 750 Gy. This level is a limitation imposed by the ProASIC3 FPGA. It is important to mention that the previously mentioned TID limit may only be achieved by applying specific design techniques for improving the radiation tolerance of the FPGA, e.g. highly pipelined FPGA firmware, reprogramming of the FPGA during operation, etc.

2.2 Optical & Electrical Interfaces

The GEFE takes advantage of the Giga Bit Transceiver (GBT)/Versatile Link platform developed by the CERN PH-ESE group. This provides a radiation hard, high-speed (4.8 Gbps), bidirectional optical link for communication with back-end electronics, and multiple low-speed (40@80 MHz, 20@160 MHz or 10@320 MHz) electrical links (e-links) for communication with digital front-end electronics. The link can be fixed and deterministic in clock phase and data latency if required. In addition to the high-speed optical link, the GEFE features a custom Electrical Serial Link Transceiver to be used in low-speed communications over copper cable through long distances (tested up to 2 km@10 Mbps). The variety of optical and electrical interfaces on the board, in addition to its flexible architecture, means that it can easily be adapted for use in many different applications where radiation tolerance is a requirement.

2.3 Upgradable

In order to maximize the versatility, the GEFE is expanded with dedicated front-end cards through a High-Pin Count FPGA Mezzanine Card (FMC HPC) connector which features up to 180 user-specific I/Os (that can be configured both as single-ended or differential pairs) as well as 4 differential clock inputs and 2 differential bidirectional clocks. The high-speed lines (DP) of the FMC HPC connector are used as user-specific I/Os and can also be used for special functions (Please note that the use of the DP lines in GEFE does not comply with the FPGA standard). In addition to the FMC HPC connector, the GEFE offers 2 general purpose connectors. Both presenting the same form-factor (26-pin ~ .050" pitch).

2.4 Flexible

The interface between the e-links and the digital front-end electronics plus enabling the different on-board connectors as well as the control of the different on-board resources (e.g. LEDs, etc.) is carried out by a Microsemi ProASIC3 flash-based FPGA, device that has been qualified for operation in radiation environments. All other components are also (or will be) qualified for use in environments with high levels of irradiation. The use of an FPGA, coupled with flexible powering, clocking and FPGA programming schemes, provides the capability to adapt the GEFE for interfacing to the user’s systems.

3. Application Examples

Motor Controller with Optical Interface (MCOD) (BE-BI-PIN)

New WorldFPGA box (CERN BE-CI)

Advanced Waterfront Experiment BPM (UNL large BPM) (CERN BE-BP)

Ultra High-Speed Analog Mezzanine Card (UHSMC) (CERN BE-CI)

BPM (Dawn)

4. Status & Outlook

The GEFE board

- Validity test of the first 2 prototypes of GEFE at (November 2015)
- Rel-Tolerance qualification of components (Second half of 2016) and full board (First half 2016)
- Pre production stage (First half of 2016) (small orders for prototyping)
- Production stage (First half of 2017)

The GEFE community

- Open Hardware Repository (OHR) Wiki and E-mail lists
- 8 projects interested so far (New NIMPOD SPS CHARM test board, New Red-Tolerant Fieldbus, etc.)
- About 50 pieces requested so far (as already fabricated)
- Contact: manuel.barron@cern.ch

Web site: http://www.ohwr.org/projects/gefe