

Bin Yang

FPGA Developer

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Rectangular Snip

Profile

- Extensive experience (7+) in developing embedded systems, including architecture, design, Xilinx / Altera FPGA, board design and SoC / ASIC
- Tools ISE / PlanAhead / Vivado / SDK, coding in VHDL / Verilog / C, script in TCL / Python
- Experience with PCIe, DDR3, SPI, I2C, AXI etc. interfaces, and High Speed logic e.g. MGT
- Implement complex IP with RTL Simulation, Verification, Synthesis, Timing closure and STA
- Capability in FPGA Design Methodology to save time and improve code reusability
- Abilities in system level multi-focus solutions
- Strong Communication Skills and Team player personality

Technical experiences

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|------------------------|---|
| May.2019- Present | Engineer: FPGA and Server Development for electron beam diagnostics Deutsches Elektronen Synchrotron (DESY), Hamburg |
| Oct.2011- Sept.2018 | Engineer: FPGA and Embedded System Development for MicroTCA Deutsches Elektronen Synchrotron (DESY), Hamburg |
| Mar.2010- Nov.2010 | Thesis: Fixed-Point Analysis of DVB-S2 Transceiver Rohde & Schwarz INRADIOS GmbH, Dresden |
| May.2009- | Internship: ATmega256 Embedded HW Development |

Education

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| Oct.2006- Jan.2011 | Diplom, Elektrotechnik- Informationstechnik Technische Universität Dresden |
| Sep.2002- June.2006 | Bachelor, Electrical and Information Engineering Tongji University, Shanghai, China |

Knowledges

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| <u>Languages</u> | German, English, Chinese |
| <u>EDV</u> | VHDL, Verilog, SystemC, SystemVerilog, TCL, Python, XML, C, matlab, SVN |
| <u>Tools</u> | <ul style="list-style-type: none">• Xilinx ISE/ PlanAhead/ SDK/ Vivado, Quartus II• Synopsys Synplify Pro/ Symphony Model Compiler• Cadence NCSIM/ Design Framework/ Encounter• Mentor ModelSim/ Questa CDC• Altium Designer, PSPICE, Eclipse, MATLAB |

Memberships and Hobby

VOE; IEEE; LLRF; Diagnostics

Travel: Reading; Sing; Symphony, Opera, Ballet
Football (Arsenal), Biking, Boating