

Power Converter Controls

**Lecture for the
CERN Accelerator School
on Power Converters**

Warrington May 16 2004

1.1 Global Controls Environment

- ◆ **Accelerators:**
 - ◆ The Advanced Photon Source (ANL)
 - ◆ The Tesla Test Facility (DESY)
 - ◆ The Continuous Electron Beam Accelerator Facility and IRFEL (TJNAF)
 - ◆ The Bates Linear Accelerator (MIT)
 - ◆ Next Linear Collider R&D (SLAC)
 - ◆ RF and feedback for PEP-II "B-factory" (SLAC)
 - ◆ The HERA cryogenic plant (DESY)
 - ◆ The Intense Pulsed Neutron Source (ANL)
 - ◆ Free Electron Laser (Budker INP)
 - ◆ The Tesla Test Facility Injector (SACLAY)
 - ◆ Racetrack Microtron (U Alabama)
 - ◆ The Free Electron Laser Program (Duke)
 - ◆ The Advanced Free Electron Laser (LANL)
 - ◆ The Average Power Laser Experiment (LANL)
 - ◆ LAMPF/LANSCE PSR (LANL)
 - ◆ LEDA (for APT) (LANL)
 - ◆ The Heavy Ion Fusion Test Stand (LBNL)
 - ◆ Advanced Light Source (*partial*) (LBNL)
 - ◆ National Laboratory for High Energy Physics B-factory (KEK)
 - ◆ Berlin Electron Synchrotron Light Source (BESSY II)
 - ◆ Microtron (U Athens)
 - ◆ RF (PSI)
 - ◆ Swiss Light Source (PSI)
 - ◆ Neutron Therapy Cyclotron (U Washington)
 - ◆ ISAA Radioactive Beam Facility (TRIUMF)
 - ◆ Magnet test facility and Accelerator R&D (Sync Lab Barcelona/IFAE)
 - ◆ SSRF synchrotron and BTCF e+/e- collider (IHEP)
 - ◆ NSRL (U Science/Tech, Hefei, China)
 - ◆ IPHI (SACLAY)
 - ◆ Spallation Neutron Source (ANL/BNL/LANL/LBNL/ORNL)
 - ◆ The National Spherical Torus Experiment (PPPL)
 - ◆ Linac Test Bed for APT (SRS)
 - ◆ Holifield Radioactive Ion Beam Facility (ORNL)
 - ◆ Cyclotron(s) Controls Upgrade (MSU)
 - ◆ DELTA Controls Upgrade (Dortmund)
 - ◆ Pohang Light Source: Longitudinal Feedback System (PAL/POSTECH)
 - ◆ Steady State Tokamak-1 (Inst. for Plasma Research, India)
 - ◆ Longitudinal Feedback for DAFNE (INFN/Frascati)
- ◆ **Detectors:**
 - ◆ Halls A, B, and C Slow Controls (JLab/NMSU)
 - ◆ Advanced Light Source Beamlines (*partial*) (LBNL)
 - ◆ Gammaphase (LBNL/ANL/ORNL)
 - ◆ Advanced Photon Source Beamlines (ANL)
 - ◆ The PHENIX detector system for RHIC Slow Controls (BNL/LANL/NMSU)
 - ◆ The STAR detector system for RHIC Slow Controls (Creighton/U. Wash/Kent State/UCLA/LBNL)
 - ◆ The Intense Pulsed Neutron Source Instruments (ANL)
 - ◆ The Biotechnology Beamline (SSRL)
 - ◆ The BaBar detector for PEP-II Slow Controls (SLAC/LBNL)
 - ◆ Structural Biology Research Group (Riken)
 - ◆ Wind Tunnels (NASA/Langley)
 - ◆ PRISMA and GARFIELD demonstrations (INFN/Legnaro)
 - ◆ D0 (FNAL)
 - ◆ High Acceptance DiElectron Spectrometer (GSI/Darmstadt)
- ◆ **Telescopes:**
 - ◆ The Gemini 8-M Telescope (AURA)
 - ◆ Kitt Peak Observatory (NOAO)
 - ◆ The United Kingdom Infrared Telescope upgrade (JAC)
 - ◆ The William Herschel Telescope/WFFOS instrument (RGO)
 - ◆ The William Herschel Telescope/ELECTRA instrument (U Durham)
 - ◆ The Keck II Telescope (CARA)
 - ◆ Canada-France-Hawaii Telescope Upgrade
 - ◆ LIGO (CalTech)
 - ◆ INTEGRAL instrument/Instituto de Astrofisica de Canarias (IAC)
 - ◆ Potsdam Multiaperture Spectrophotometer (Astrophysical Inst)
 - ◆ Sloan Digital Sky Survey/Telescope Performance Monitor (SDSS)
- ◆ **Commercial:**
 - ◆ The High Power Laser Experiment (Boeing)
 - ◆ Wafer Fabrication Plant (AMD)
 - ◆ Liquefied Nature Gas Plant (Baltimore G&E)
 - ◆ Tunnel Fire Ventilation Test Program (DOT/Bechtel-Parsons-Brinkerhoff)
 - ◆ Flexible Manufacturing Facility (Allied Signal)
 - ◆ Wastewater Treatment (Western Lake Superior Sanitary District)
 - ◆ Potable Water Distribution (St. Louis County)
 - ◆ Compressor Control (Baltimore G&E)
 - ◆ GM Fuel Cell Program (LANL)
 - ◆ Plant Simulation (Knolls)
 - ◆ Flight Simulation (JPL)
 - ◆ Fuel Depots (US Navy)
 - ◆ Product Storage/Movement Facility (Citgo)
 - ◆ Ground Tracking Station (NASA Canberra)
 - ◆ Well Head/Extraction (Saphania Oil Field)
 - ◆ Superconducting Magnet Test Facility for KSTAR (Samsung Adv. Inst. of Tech.)

1.2 Global Controls Environment

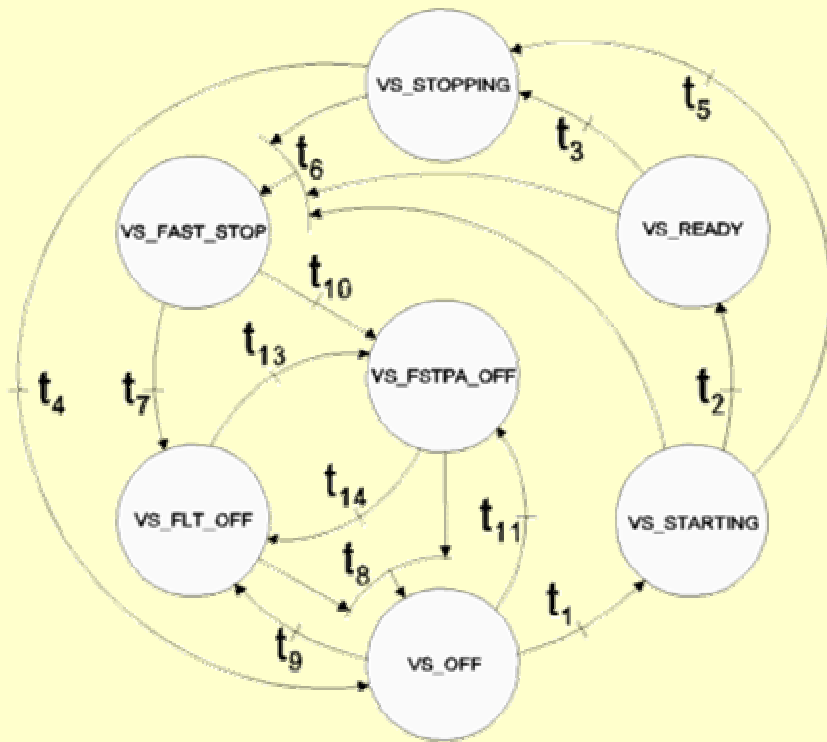
- ◆ Normally imposed by project
- ◆ EPICS
 - ◆ Many major projects worldwide
 - ◆ Excellent for new projects
 - ◆ All or nothing so difficult with existing projects
- ◆ Other SCADA systems - not really suitable

2.1 Homemade verse COTS

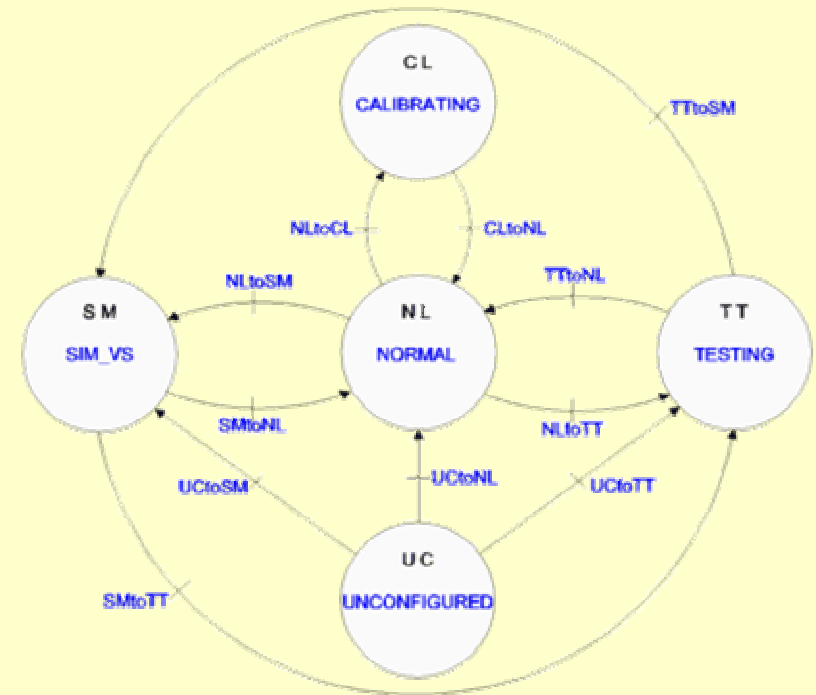
- ◆ **Work out your requirements**
- ◆ **Identify your priorities**
- ◆ **Consider constraints**
- ◆ **Consider options:**
 - ◆ **PLCs**
 - ◆ **Mixed system based on COTS bus**
 - ◆ **Dedicated home made system**
- ◆ **Make your decision and good luck!**

3.1 Power Converter State Management

Voltage Source State



Operational State



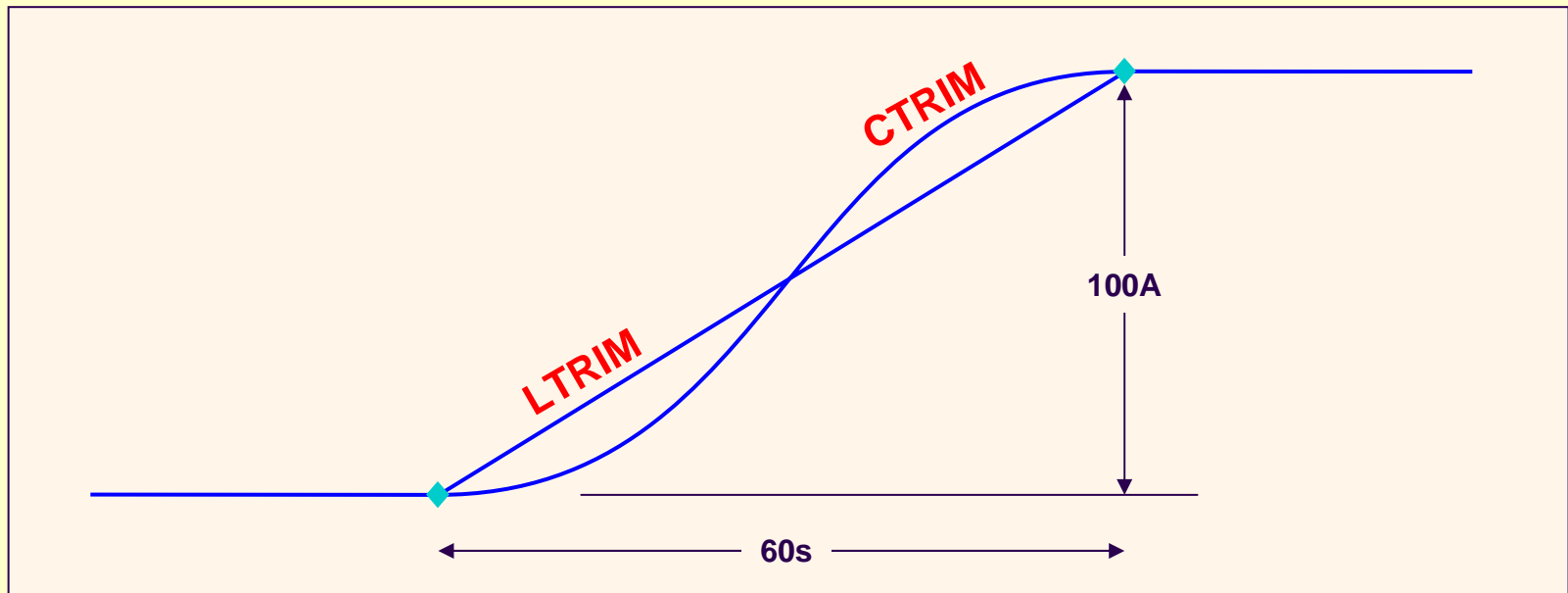
3.3 Power Converter State Management

- ◆ Design your state machine(s)
- ◆ Identify status and command signals required for each transition
- ◆ Choose your signal types
 - ◆ $< 500\text{mV CM}$ – direct connection
 - ◆ $< 10\text{V CM}$ – differential connection
 - ◆ $< 1500\text{V CM}$ – Opto or capacitive couplers or relays
 - ◆ $> 1500\text{V CM}$ – Fibre
 - ◆ **Ensure safe behavior if the cable is removed**

4.1 Function Generation

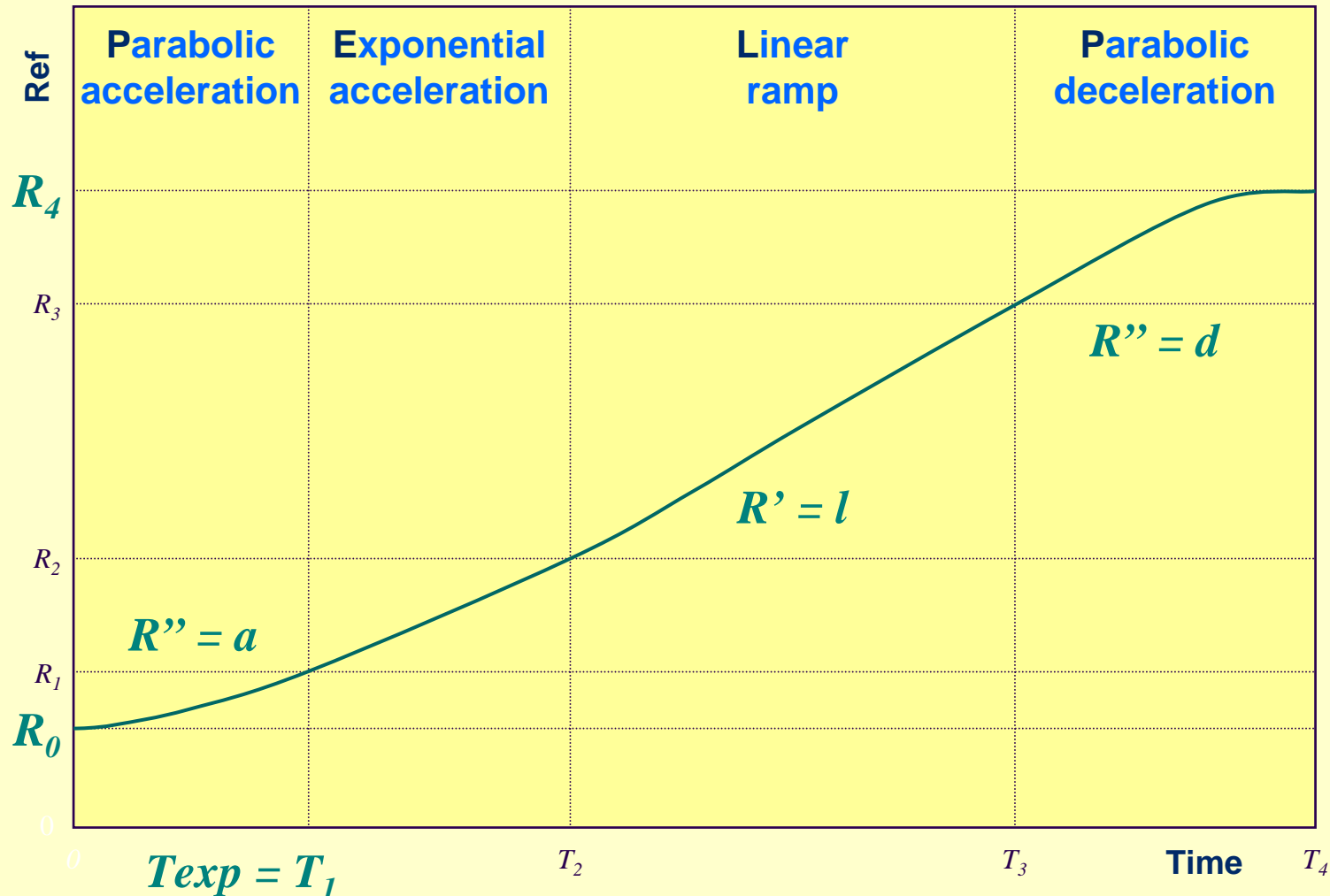
Parametric functions

Linear Trim and Cubic Trim



4.2 Function Generation

Parametric functions: PP, PLP, PEP, PELP, PLEP



4.3 Function Generation

Real-time control: NONE, SUM, GAIN, RT ONLY

$$\text{ref} = R(t)$$

$$\text{ref} = R(t) + R_{rt}$$

$$\text{ref} = R(t) \cdot (1 + R_{rt})$$

$$\text{ref} = R_{rt}$$

4.4 Function Generation

- ◆ **Identify your requirements**
- ◆ **Use linear interpolation**
- ◆ **Use parametric function**
- ◆ **Support real-time control**
- ◆ **Use engineering units (Amps or Volts)**

5.1 Network

- ◆ **Define your overall architecture (2 or 3 layers?)**
- ◆ **Choose your media: Ethernet, Profibus, WorldFIP, etc...**
- ◆ **Considering:**
 - ◆ **Chipset cost/complexity**
 - ◆ **Software overhead – IP or private protocol**
 - ◆ **Cabling and connector costs**
 - ◆ **Performance: max length, number of nodes, repeaters, through put**
 - ◆ **Radiation tolerance if required**
 - ◆ **Real time support (control, publishing, synchronisation)**

6.1 Synchronisation

- ◆ **Identify your requirements**
- ◆ **Review your timing environment**
- ◆ **Use data network for timing if possible**
- ◆ **Use a digital PLL to generate RT clock in embedded systems**

7.1 Regulation

- ◆ **Use digital current regulation unless the requirements are very undemanding**
 - ◆ **Software can control the loop parameters**
- ◆ **Have an independent measurement of the current**
 - ◆ **Two DCCTs, two ADCs**

8.1 Analogue Acquisition

- ◆ Precision analogue electronics is hard
- ◆ Don't try it unless you have the right competence and lots of patience
- ◆ COTS can be crap – believe nothing - test everything
- ◆ The whole design matters: Vrefs, ADCs, layout
- ◆ Filter appropriately - know your noise environment

9.1 Mechanical Issues

- ◆ **Very important to reliability – don't underestimate the problem**
- ◆ **Casings should be robust, provide EMC protection**
- ◆ **Check thermal behaviour – avoid fans if possible**
- ◆ **Choose connectors very carefully**
- ◆ **Avoid ambiguous connectors**
- ◆ **Avoid intermediate cabling**

10.1 Inventory Management

◆ Barcode

- ◆ Materials are complex – choose carefully
- ◆ Printer is a specialised (expensive) device
- ◆ Scanners – wide choice – Serial, USB, Wireless, Laser, CCD

◆ Dallas 1-wire bus

- ◆ Identity and optional temp sensors available
- ◆ Separate bus using 2 wires (data/power and ground)
- ◆ No position information

11.1 Remote Management and Diagnostics

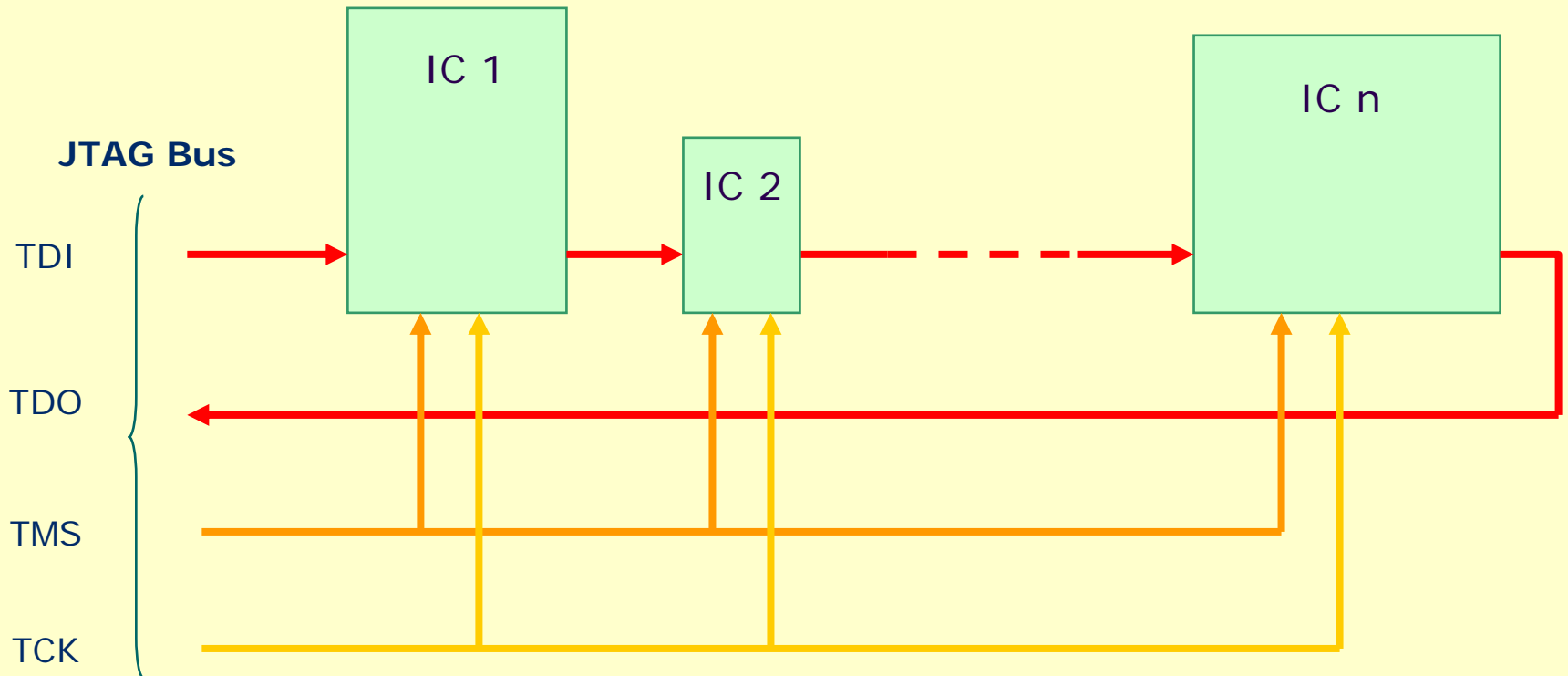
- ◆ Invest according to scale and remoteness
- ◆ Validate controller – then diagnose power converter
- ◆ First fault detection is very important
- ◆ Consider remote logic download
- ◆ Include remote code download
- ◆ Include remote parameter download

12.1 Power Supplies

- ◆ **Work out all your requirements**
- ◆ **Consider your powering environment**
- ◆ **Decide on your topology**
- ◆ **Remember to add a switch and status signals**

13.1 Testing

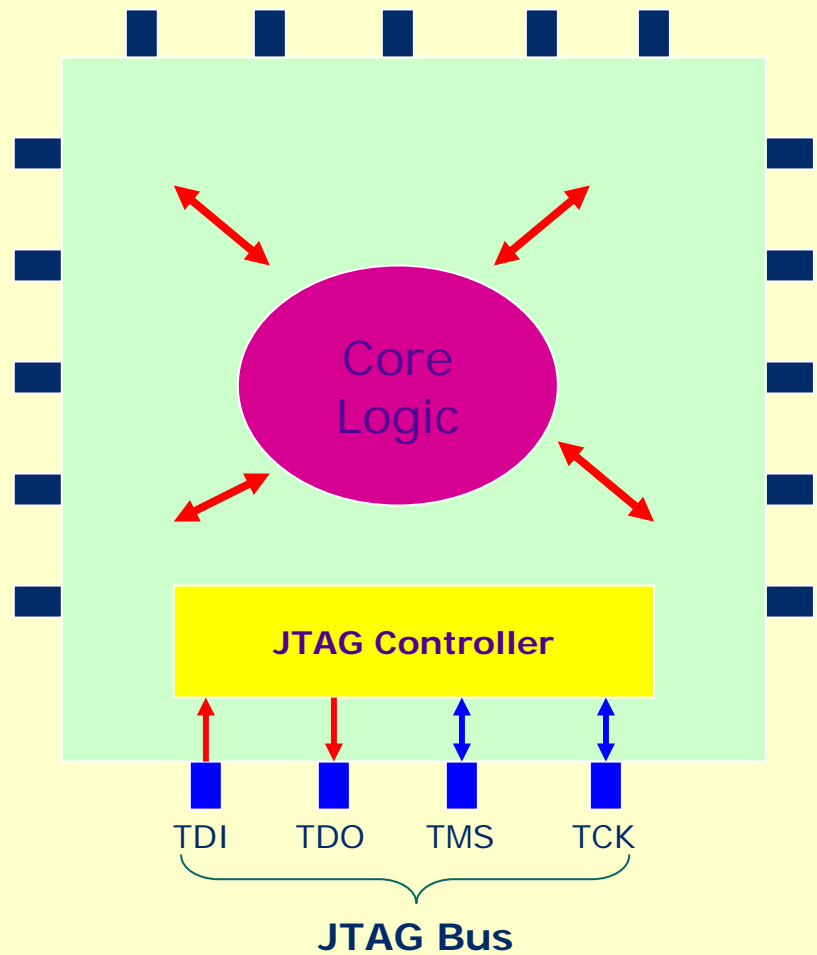
JTAG Boundary Scan: The JTAG bus



13.2 Testing

Normal device operation:

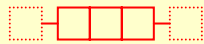
- Core logic controls pins
- JTAG controller is passive



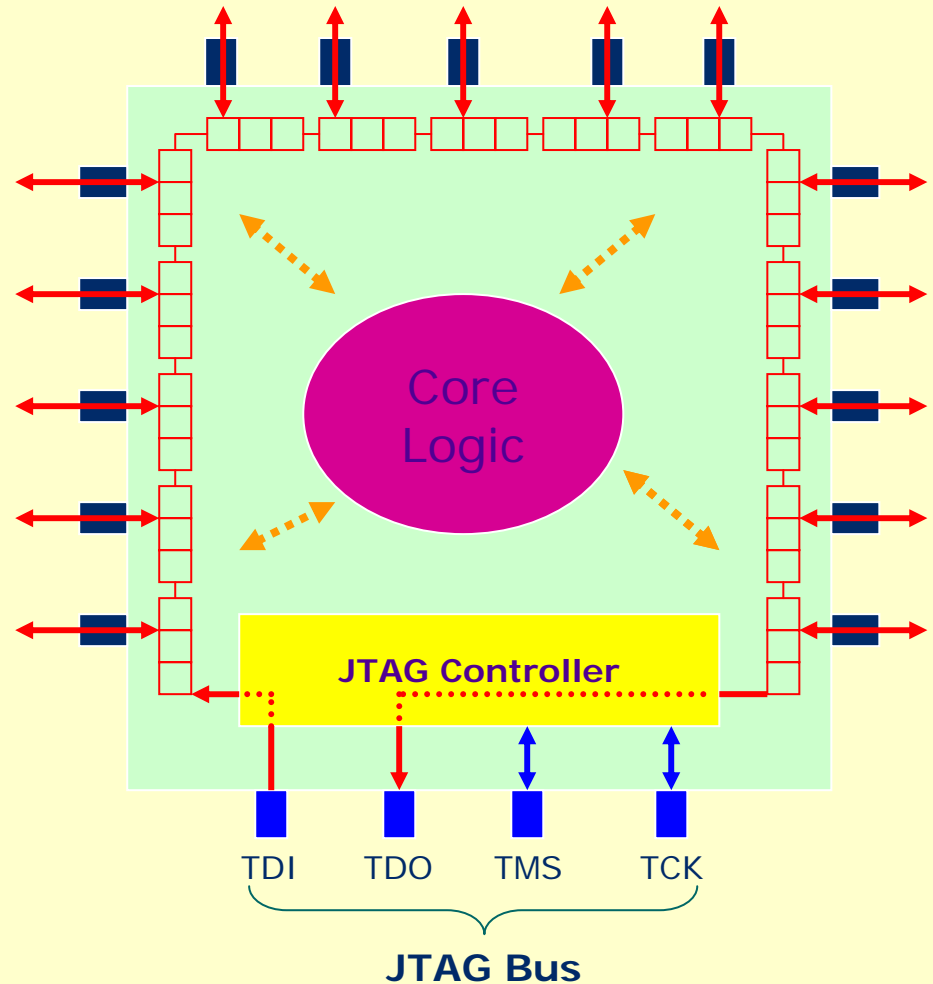
13.3 Testing

Boundary Scan Mode:

- Core logic disconnected from pins
- JTAG controller controls pins via daisy chain of boundary scan registers

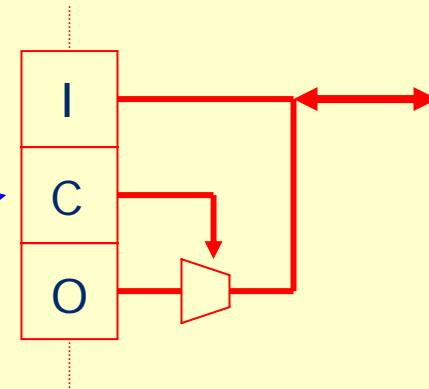
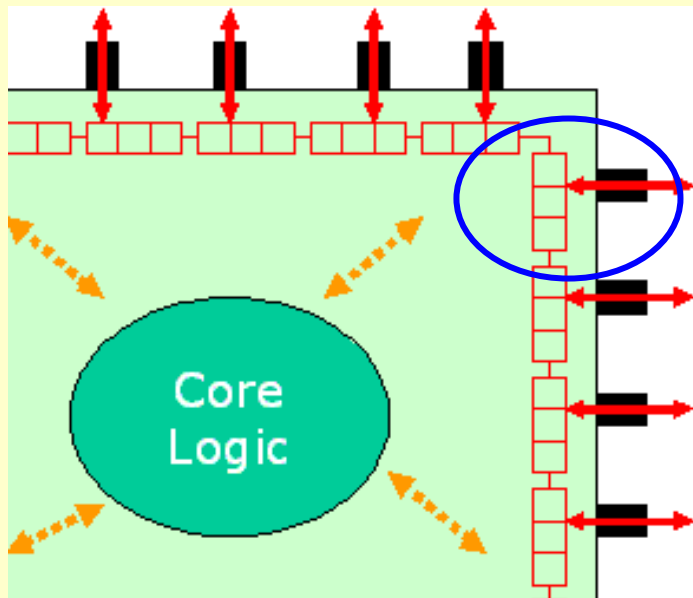


Boundary Scan Register



13.4 Testing

JTAG Boundary Scan Registers



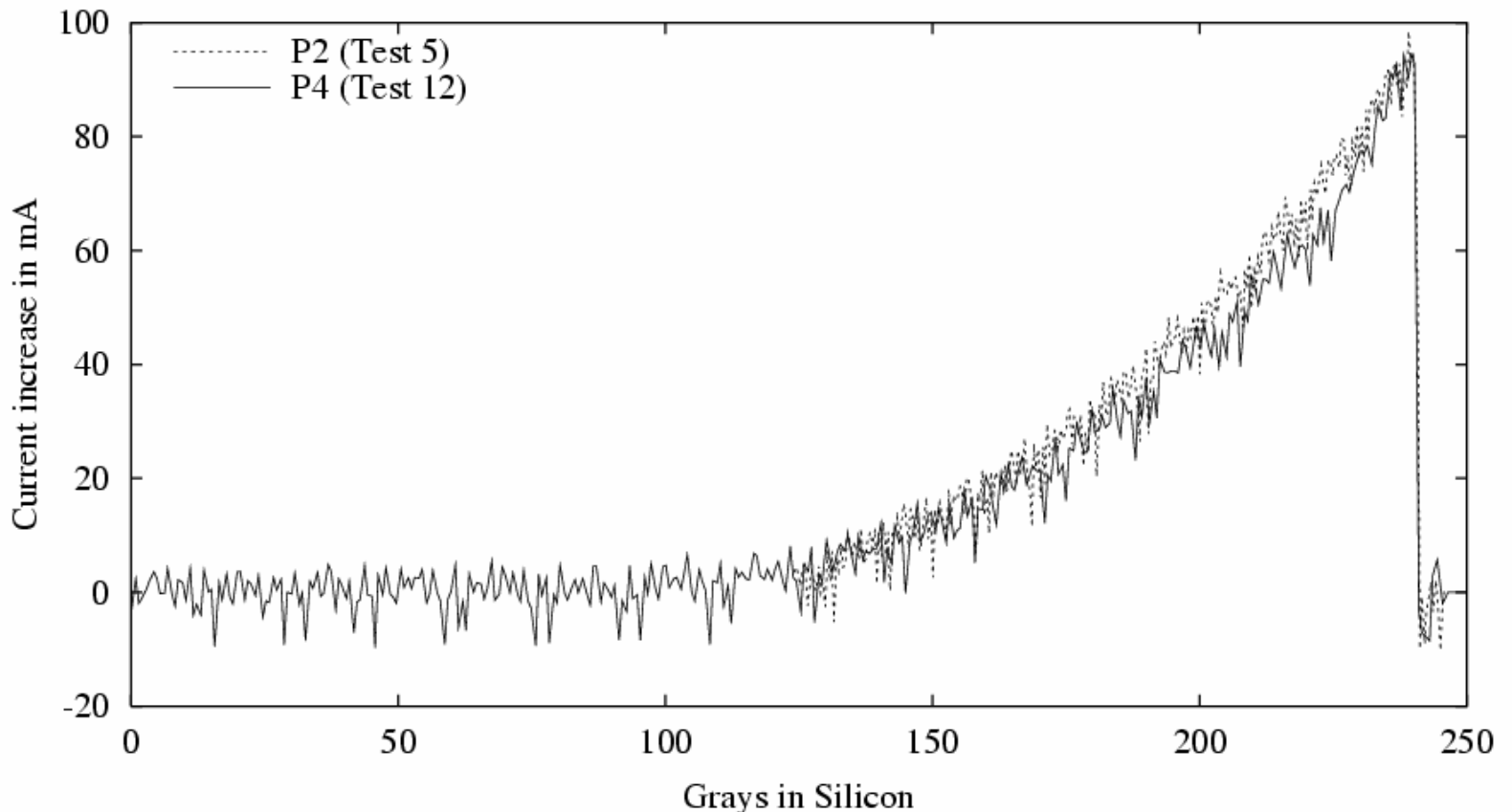
- 3 Boundary scan registers per pin:
- 1 bit per registers (0 or 1)
 - I = Input register
 - C = Control register (Input or output)
 - O = Output register

13.5 Testing

- ◆ **Make automatic test equipment for production and repair – lots of work**
- ◆ **Three levels of testing – DLI**
- ◆ **Design for Test – DTF**
- ◆ **Use JTAG boundary scan for in-situ testing**
- ◆ **Anticipate obsolescence**

14.1 Radiation

Figure 9: CPU CPLDs current increase against dose



14.2 Radiation

- ◆ **<100 Grays is relatively easy with COTS**
- ◆ **100-200 Grays still feasible with careful choice of COTS components**
- ◆ **Above 200 Grays is difficult**
- ◆ **Above 1000 Grays is VERY expensive**
- ◆ **EDAC memory works**
- ◆ **Crashes inevitable and must be managed**
- ◆ **Latch-ups require a power cycle**

15.1 Protocols

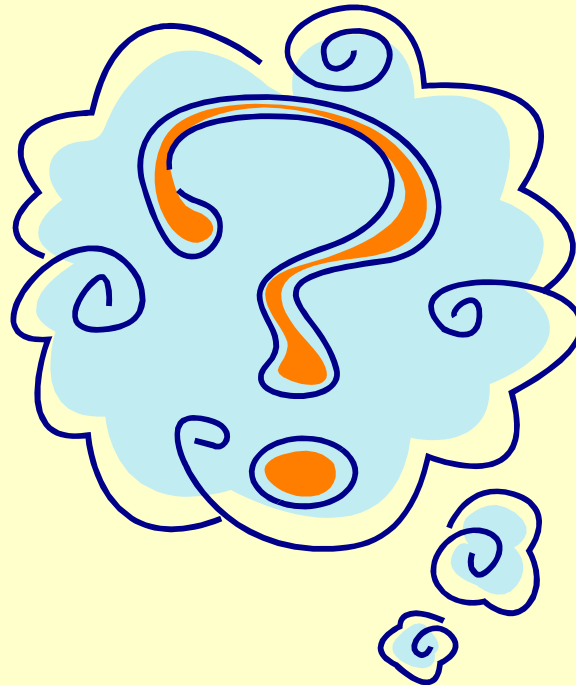
- ◆ **Use ASCII for commands and responses**
- ◆ **Allow low level access with dumb terminal**
- ◆ **Allow non-blocking communication**
- ◆ **Acknowledge all commands**
- ◆ **Support Set and Get only**
- ◆ **Avoid JAVA and C++ in embedded systems**

16.1 Documentation

- ◆ **Golden rule of Data: define everything only once**
- ◆ **Use XML syntax**
- ◆ **Parse your XML into everything you need including documentation**
- ◆ **Exploit the web**
- ◆ **Remember to archive all your datasheets**

The End

Thanks for listening!



Any questions?