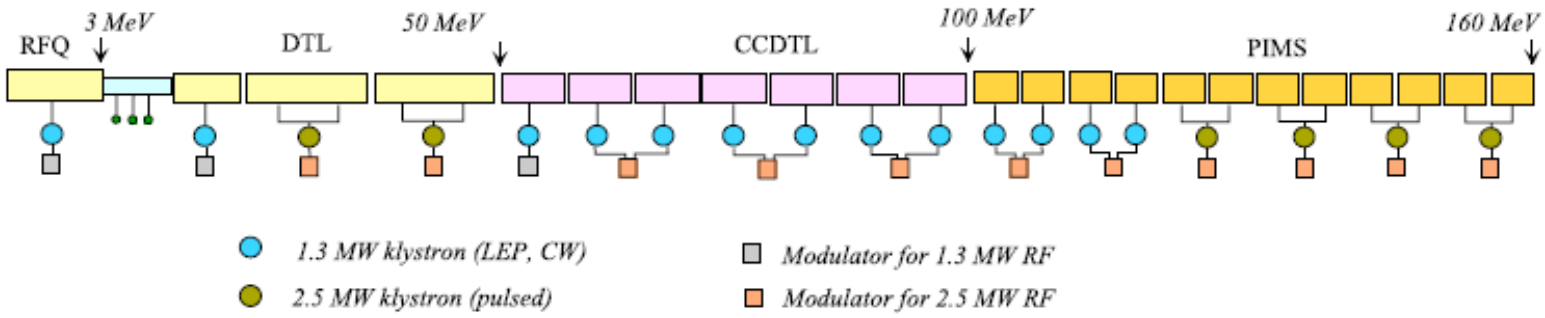
Low Level RF
Part 3: Implementation

8. Design Example: Linac4
   - Presentation of Linac4
   - Cavity Controller Functionalities
   - Architecture
   - Modeling
   - Hardware
   - A few Key Building Blocks
   - PCBs
   - Installation

CAS RF

P. Baudrenghien CERN-BE-RF

Linac4



- 160 MeV H^- Pulsed Linac
- PSB injector
- 40 mA average current (nominal)
- Normal Conducting cavities, 352.2 MHz operation
- ~ 1 MW/cavity (except DTL2 and DTL3 ~ 2 MW/cavity) with 40 mA
- 2 Hz rep rate
- Commissioning in 2013. Injection in PSB in 2015
- Proposed LLRF is much inspired from SNS

20-30% klystron power margin for regulation

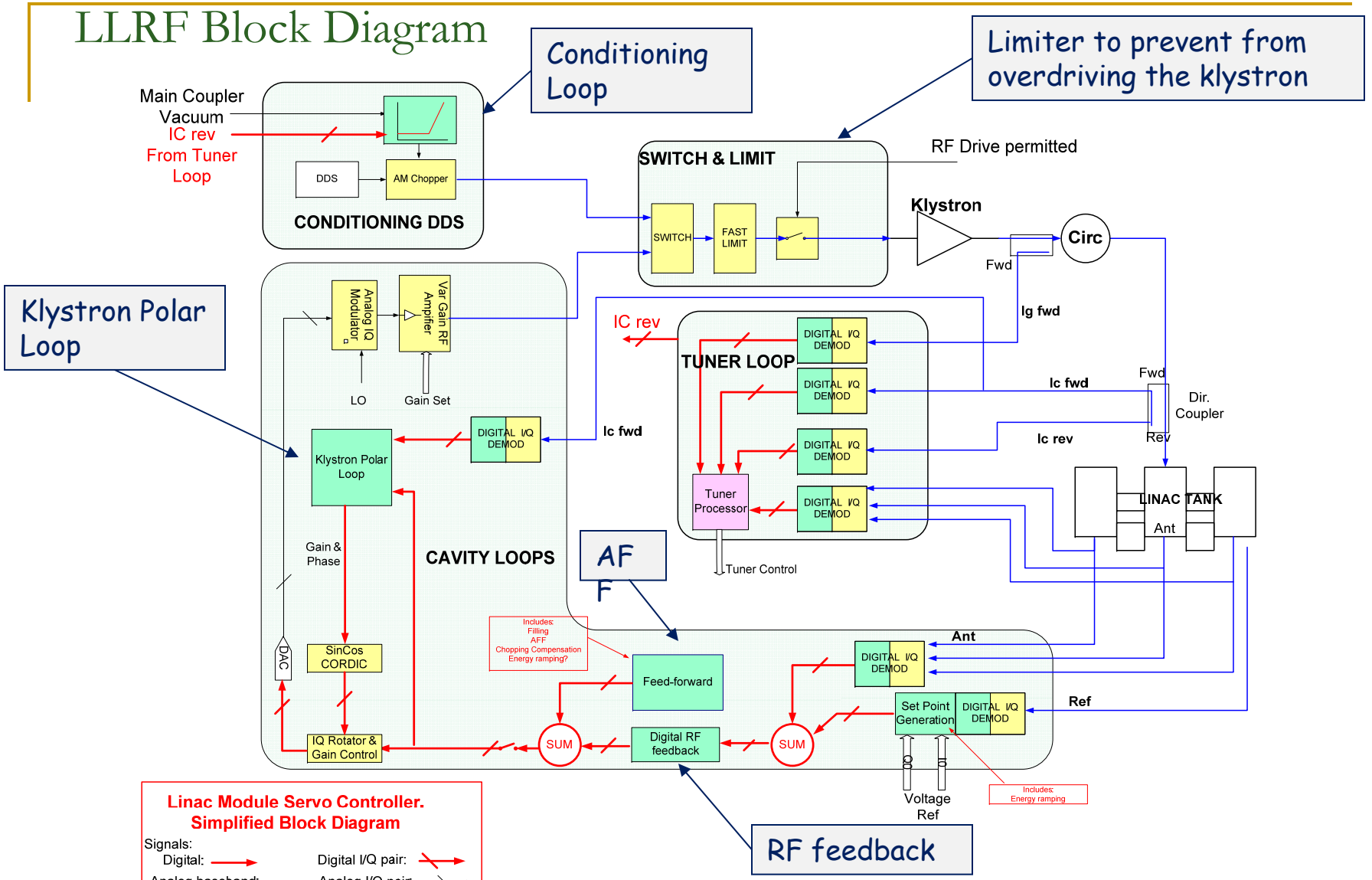
Cavity Controller Functionalities

For each cavity:

- A Tuner Loop to keep the structure on resonance
- An RF Feedback, and an Adaptive Feedforward (AFF) to keep the accelerating voltage at the desired value in the presence of beam transient
- A Klystron Polar Loop to compensate the variation of klystron gain and phase shift caused by High Voltage (HV) supply fluctuations and droop
- A Conditioning System monitoring the Cavity Vacuum while feeding the Line with Frequency Modulated bursts of RF power of increasing amplitude
- A Klystron Drive Limiter that prevents from driving the klystron over the saturation limit during loop transients.

Architecture

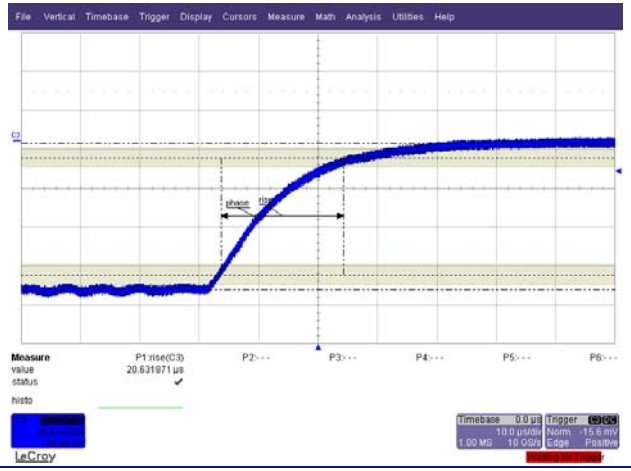
LLRF Block Diagram



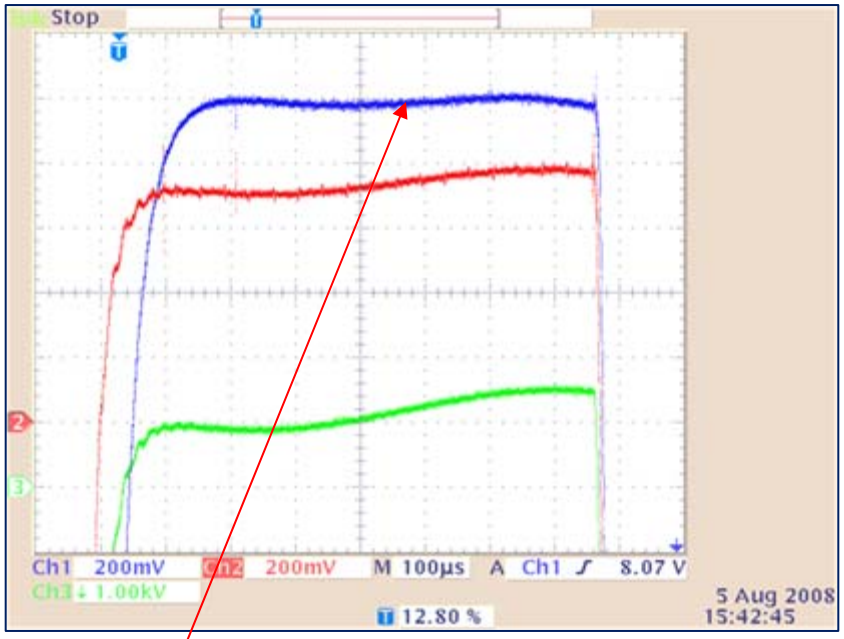
Version: 20100524

Klystron Loop

- Klystron HV pulse
  - Flat-top 1.2 ms
  - Precision 1%
  - Ripple 0.1 %
- LEP klystron:
  - 1 % HV -> 8.4 degree phase shift @ RF
- Linac4 Klystron loop:
  - Expect < 50 μs risetime



LHC: Klystron loop phase response, 20 μs risetime

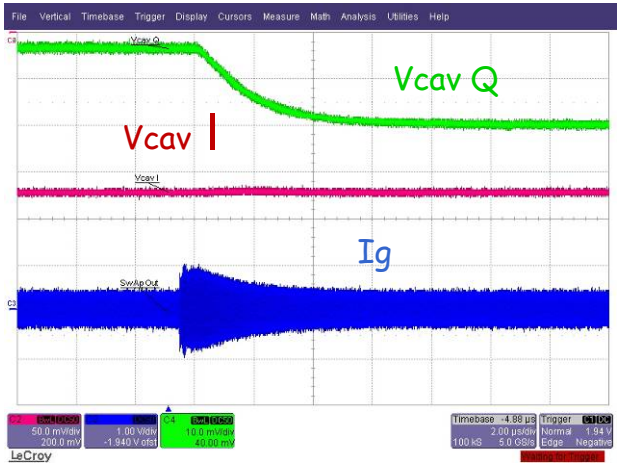


3 MeV Test Stand. RF Off. Pulsing the P.S: 100 kV/23 A at 2 Hz rate. Zoom at flat-top: Ch1 – Cathode voltage (2kV/div) ; Ch2 – Cathode current (0.8A/div) ; Ch3 – Anode voltage to ground (1 kV/div).

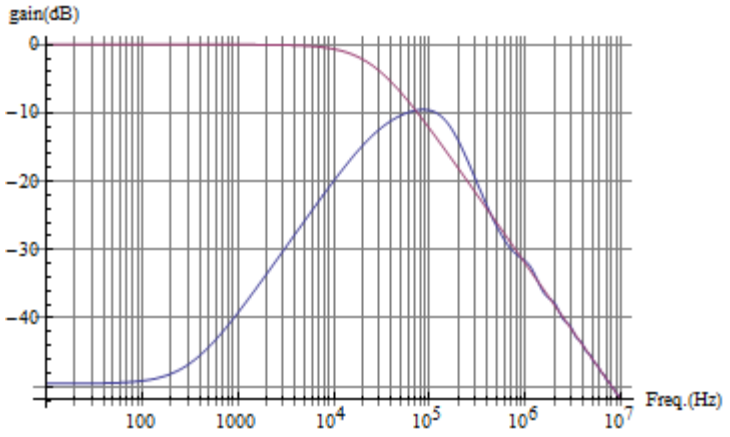
- Improved PS understudy
  - Reduced ripples…but at higher frequency
  - Simulations must tell whether it is desirable.
- HV ripple hopefully reduced by AFF if synchronized with rep rate

RF feedback

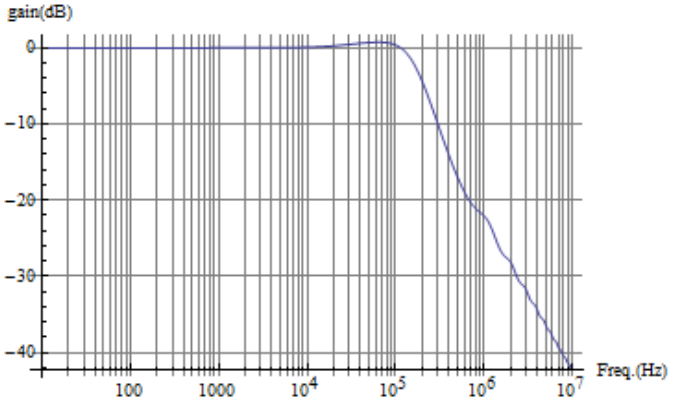
- Loop Delay: 1100 ns
  - 160 m Cable/Waveguide=550 ns
  - Klystron 250 ns
  - Circulator 50 ns
  - Driver 50 ns
  - LLRF 200 ns
- With Fdbk Closed we expect
  - ~ 150 KHz single-sided Loop bandwidth
  - <10 μs response time



LHC: 100 kV in 3 μs, 2 μs per div, T=650 ns
Linac4 reaction should be two times slower

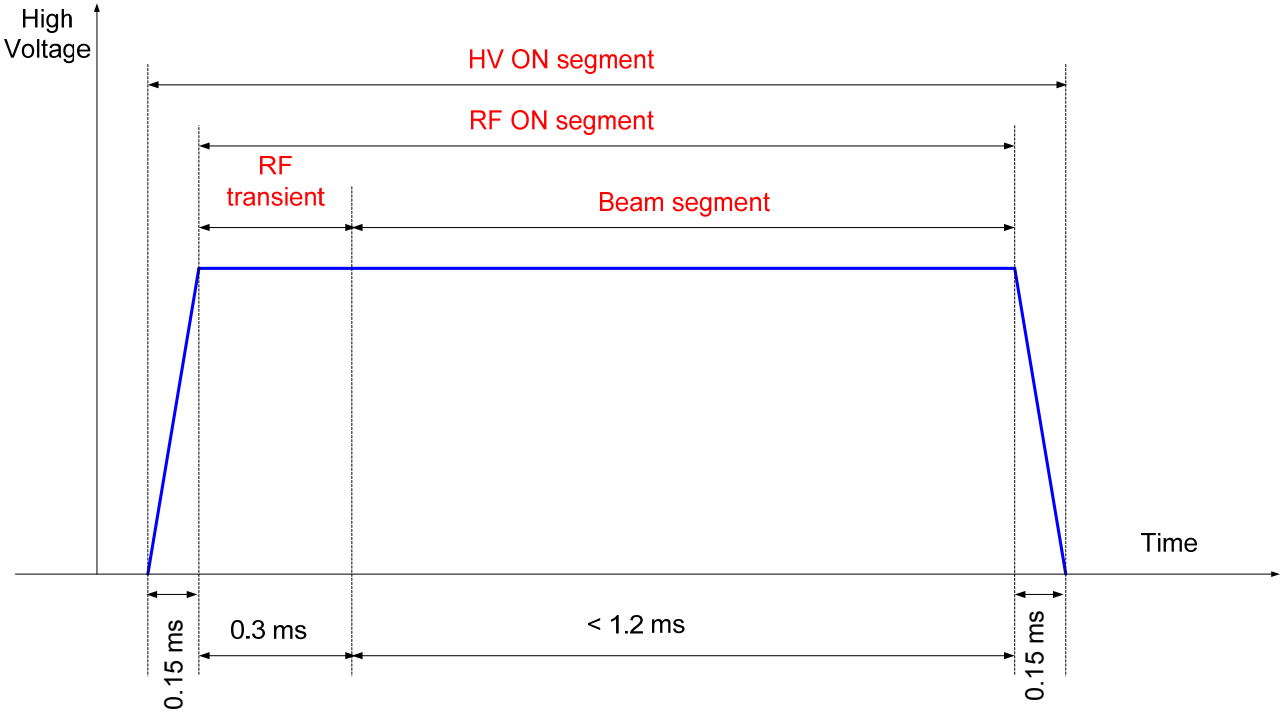


PIM: Cavity impedance without feedback, QL=7000 (red) and with PI feedback (blue) .P gain ~3.



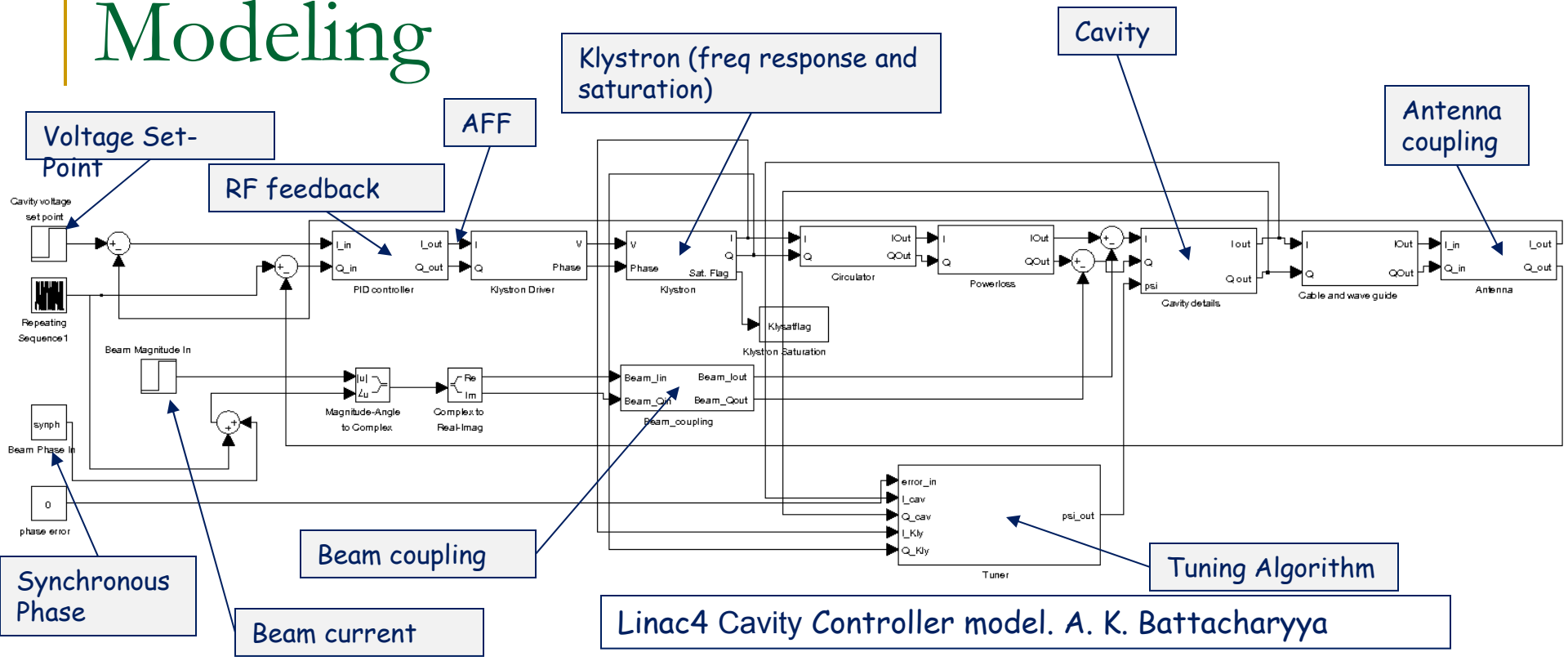
Closed Loop response with PI RF feedback. Same as above. Single-sided -3 dB BW ~ 150 kHz

Pulsing



- The beam pulse is 400 μs long but it can be later extended to 1.2 ms
- We have 300 μs for LLRF loops stabilization. We will use a sequence as at SNS
  1. Filling of the cavity open-loop but with feedforward from the result of the previous pulses. Cavity filling time < 20 μs (Q_L<20k)
  2. Switch the RF feedback ON. Ramp fdbk gain. Allow ~ 100μs for stabilization.
  3. Switch the AFF ON and the Chopping Compensation ON
  4. Beam ON
- 2 Hz rep rate

Modeling



- Step 1: Is the klystron power sufficient for the intended voltage/phase manipulations (set point)?
- Step 2: Coarse adjustment of the loop parameters (Feedback, Klystron Polar Loop, AFF) to keep the ensemble "well behaved"
- Step 3: Introduce perturbations: klystron noise, beam loading, source current ripples. Derive expected field stability. Optimization of the algorithms. Modifications to other parts of the machines: Power Converter, source, beam current, voltage distribution among the structures (beam dynamics)…

If interested, contact Anirban Krishna Battacharyya, present at the course

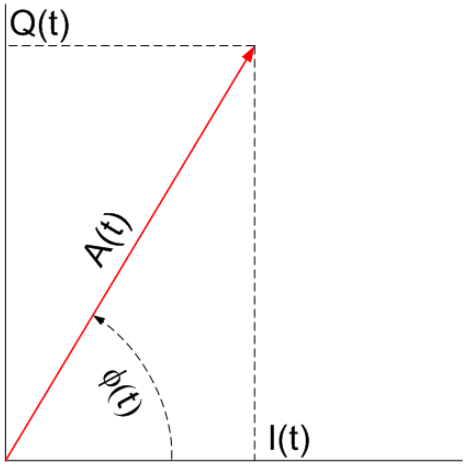
Hardware

Digital I/Q Demodulator

- In a feedback system with high loop gain, the quality of the measurement front-end sets the quality of the ensemble: In the frequency band where the loop gain is high, the LLRF will adjust the klystron drive so that the Measured Cavity Field is equal to the set-point. Measurement error will be directly reflected in the cavity field
- In large Synchrotrons and Linacs, the RF frequency is too high to allow for direct sampling of the cavity field and waveguide coupler signals. But the needed BW is typically very small as the signals come from narrow-band elements such as cavities or klystrons
- A typical front-end will therefore contain a Mixer that shifts the RF signal to an IF frequency that can be conveniently sampled by an ADC
- Amplitude/phase loops can be used in low current machines. In a high beam loading configuration they become unstable and (I,Q) implementations are preferred

- We consider a narrowband signal V(t) (cavity field for example) at the RF frequency. It can be represented either in polar (A,ϕ), or cartesian (I,Q) notations

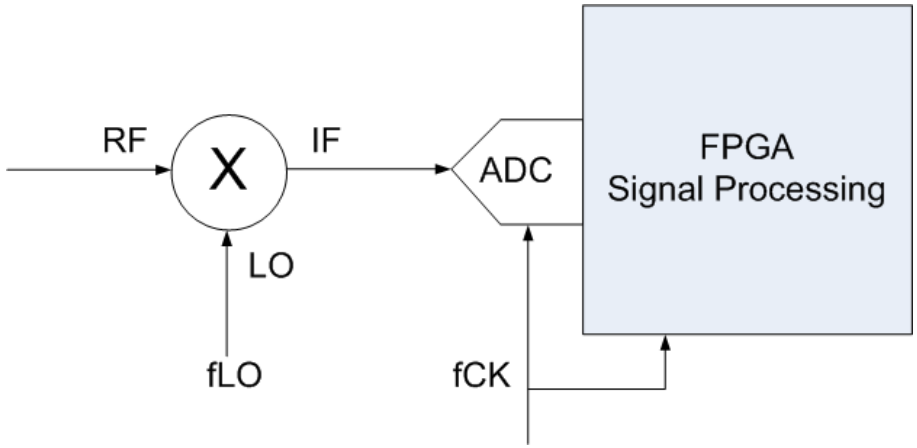
$$V(t) = A(t)\sin\left(2\pi\ f_{RF}\ t + \phi(t)\right) = I(t)\sin\left(2\pi\ f_{RF}\ t\right) + Q(t)\cos\left(2\pi\ f_{RF}\ t\right)$$



- Amplitude A(t), phase ϕ(t) and cartesian coordinates (I(t),Q(t)) are slowly varying signals. Their BW is much smaller than the RF frequency. They are related by

$$I(t) = A(t)\cos\ \phi(t)$$
$$Q(t) = A(t)\sin\ \phi(t)$$

I/Q Sampling



$$f_{IF} = f_{RF} - f_{LO}$$
$$f_{CK} = 4\, f_{IF}$$

- The RF signal is shifted to the IF frequency band using a mixer

$$V_{RF}(t) = A(t)\sin\left(2\pi\, f_{RF}\, t + \phi(t)\right)$$
$$V_{IF}(t) = A(t)\sin\left(2\pi\, f_{IF}\, t + \phi(t)\right)$$

- The sampling frequency is chosen to be four times the IF. Let x_n be the sampled signal, with n the time index, we get

$$x_n = A(nT_{CK})\sin\left(2\pi\, n\, f_{IF}\, T_{CK} + \phi(nT_{CK})\right)$$
$$x_n = A_n \sin\left(n\frac{\pi}{2} + \phi_n\right)$$

$$x_n = (-1)^{\frac{n}{2}} A_n \sin(\phi_n) = (-1)^{\frac{n}{2}} Q_n \qquad \text{for n even}$$
$$x_n = (-1)^{\frac{n+1}{2}} A_n \cos(\phi_n) = (-1)^{\frac{n+1}{2}} I_n \qquad \text{for n odd}$$

- The demodulator generates the data $\{Q_0,-I_1,-Q_2,I_3,Q_4,\ldots\}$ from which we derive, after sign correction and decimation, the data flow $\{(I_n,Q_n)\}$ at the rate $f_{CK}/2$
- Note that the I and Q are measured at alternate samples. The decimation introduces an error that increases with frequency. The I/Q demodulator is therefore narrow-band
- For Linac4 we use

$$f_{RF} = 352.2\ \text{MHz}$$
$$f_{LO} = 330.1875\ \text{MHz}$$
$$f_{IF} = 22.0125\ \text{MHz}$$
$$f_{CK} = 88.05\ \text{MHz}$$

  and we get an (I,Q) pair at 44.025 MHz rate that we interpolate to do the Signal Processing at the full 88.05 MHz FPGA clock
- Except for its narrow BW, the I/Q demodulator has many advantages: The effect of ADC offset can be nulled. The ADC gain is not critical as I and Q are affected in the same way. For slow applications (tuning for example), the very large oversampling leads to extremely good SNR after decimation.
- It was first proposed for PEP2 [Ziomek]. It is now used most everywhere…
- Much more on I/Q Demodulator in *CAS Digital Signal Processing, June 2007, T. Schilcher, RF Applications in digital signal processing*

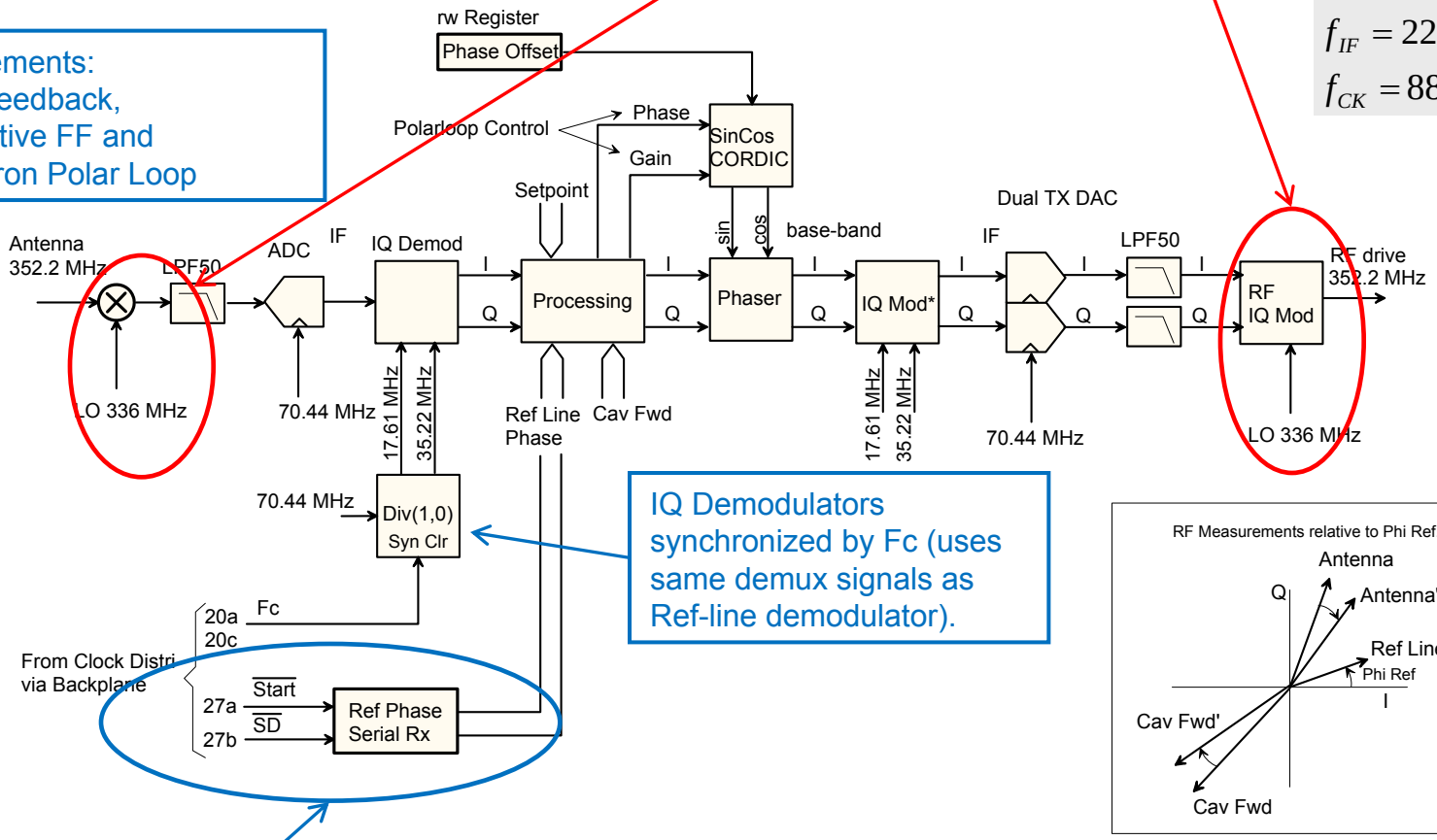
[Ziomek] C. Ziomek, P. Corredoura, Digital I/Q Demodulator, PAC95

Cavity Loops Module

System Independent of LO phase

$f_{RF} = 352.2\ \text{MHz}$
$f_{LO} = 330.1875\ \text{MHz}$
$f_{IF} = 22.0125\ \text{MHz}$
$f_{CK} = 88.05\ \text{MHz}$

Implements:
RF Feedback,
Adaptive FF and
Klystron Polar Loop



IQ Demodulators synchronized by Fc (uses same demux signals as Ref-line demodulator).

De-serialized Reference-line RF Phase used to normalize the phase of the RF Measurements.

IQ Mod* Iout = Iin * cos(x), [1, 0, -1, 0]
Qout = Qin * sin(x), [0, 1, 0, -1]

EDA-0xxxx	Title	RF Feedback Linac4 Principle	Page	1/1
CERN	Designer	John C. Molendijk BE/RF/cs		
	Date	2010/06/01	Version	1.0

Courtesy of John Molendijk

A few
Key Building Blocks

For more info on this subject, contact:

John.Molendijk@cern .ch

or

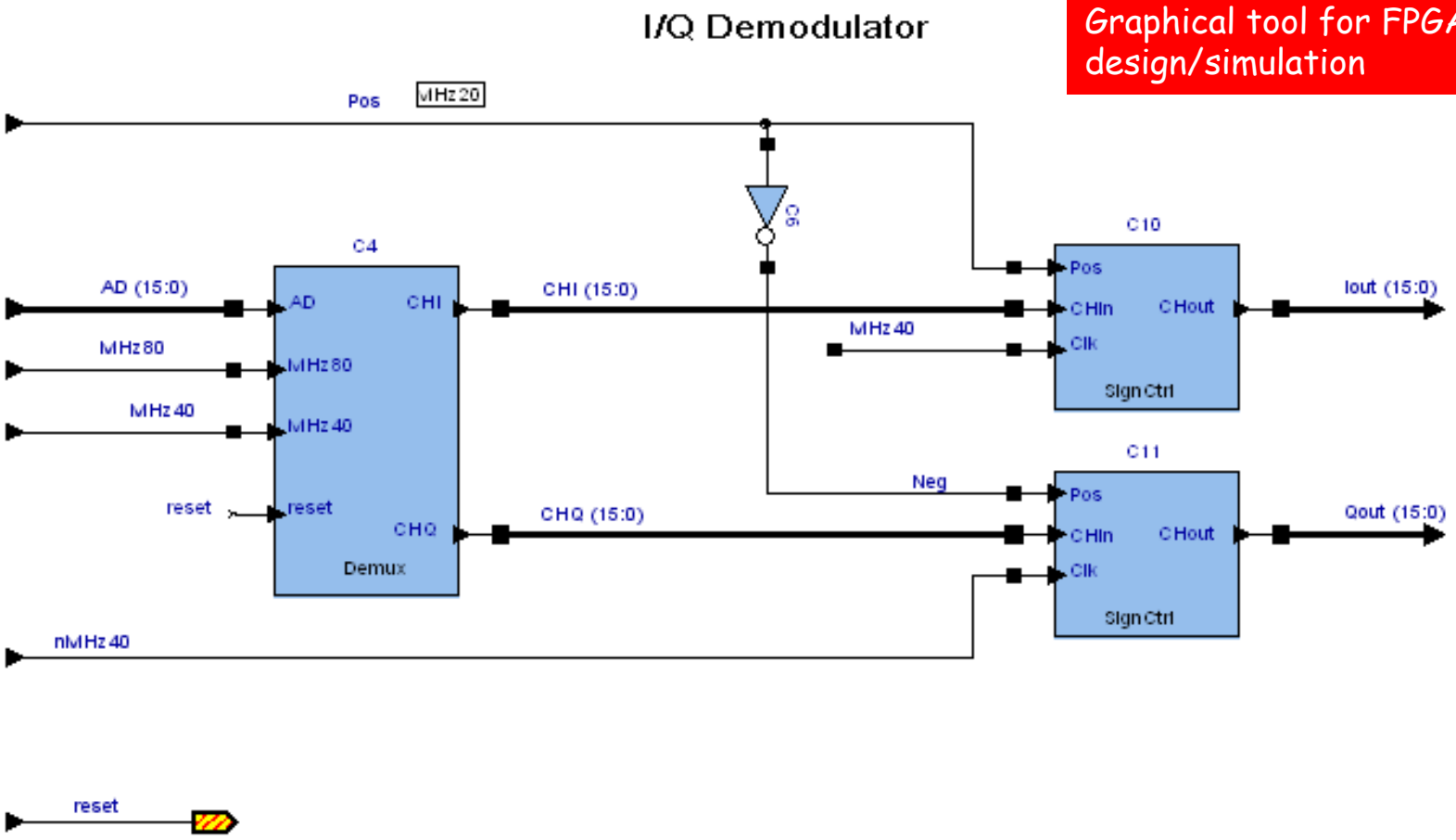
Gregoire Hagman and Jose Noirjean, present at this course

FPGA design and Visual Elite

- Signal Processing in FPGA
  - Fixed Point Arithmetic
  - Caution: scaling to avoid overflow but preserve SNR
  - Use embedded fixed point multipliers
  - Much “inspiration” from *U. Meyer-Baese, Digital signal Processing with Field Programmable Gate arrays, Sringer Verlag, 2001*
- Design with Visual Elite. Advantages:
  - Generates Device independent portable VHDL code.
  - Code reusability
  - Graphical Interface. Accept State-Diagram, Truth Tables, Processing Blocks (Adder, Logics, Multiplier, Memory) or VHDL code
  - Hierarchical
  - Graphics to text, text to graphics conversion
  - Powerful auto-documenting creates html

Digital I/Q Demodulator

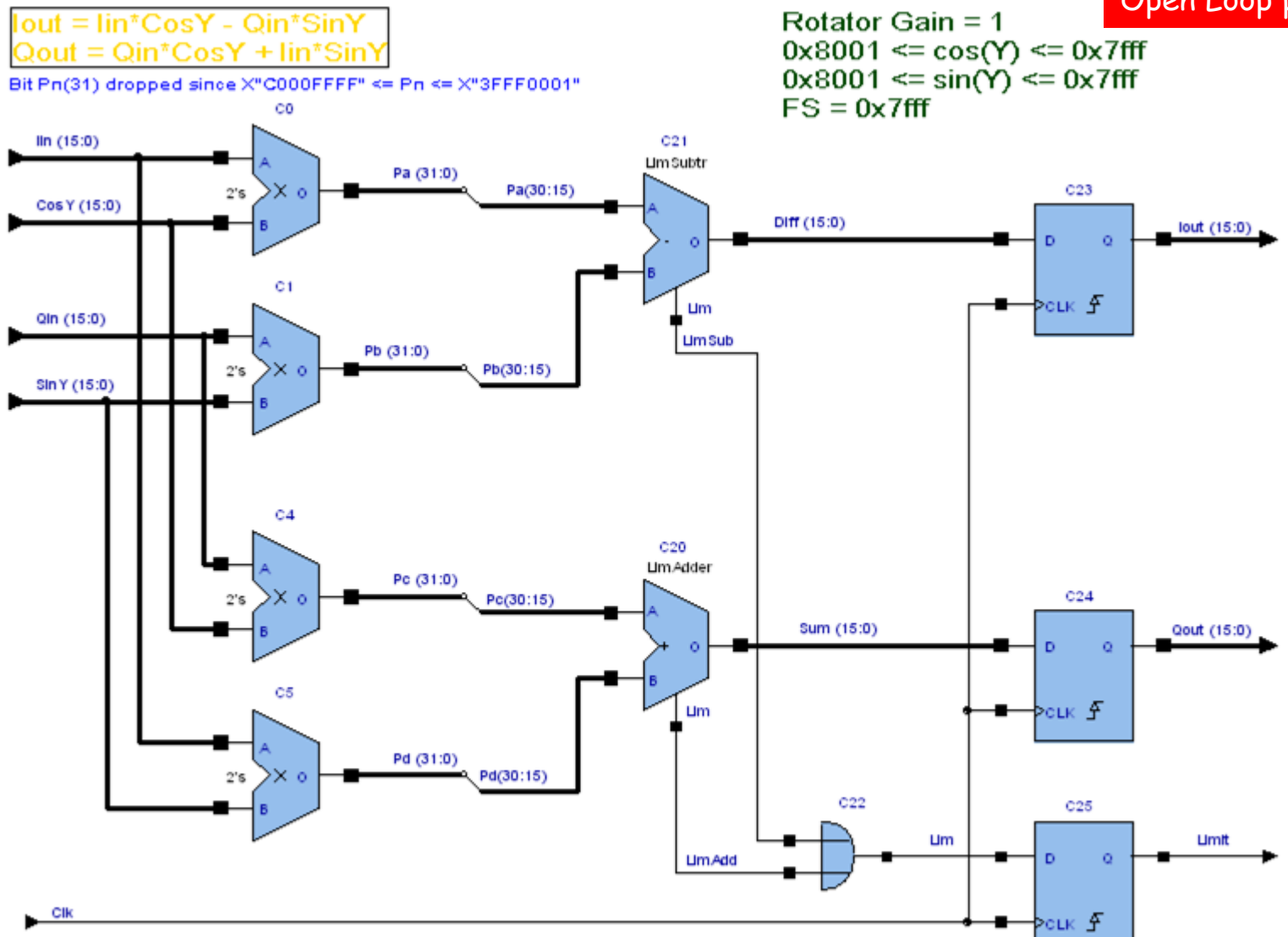
Visual Elite
Graphical tool for FPGA design/simulation



Courtesy of John Molendijk

Phase Rotator

Used to adjust Open Loop phase



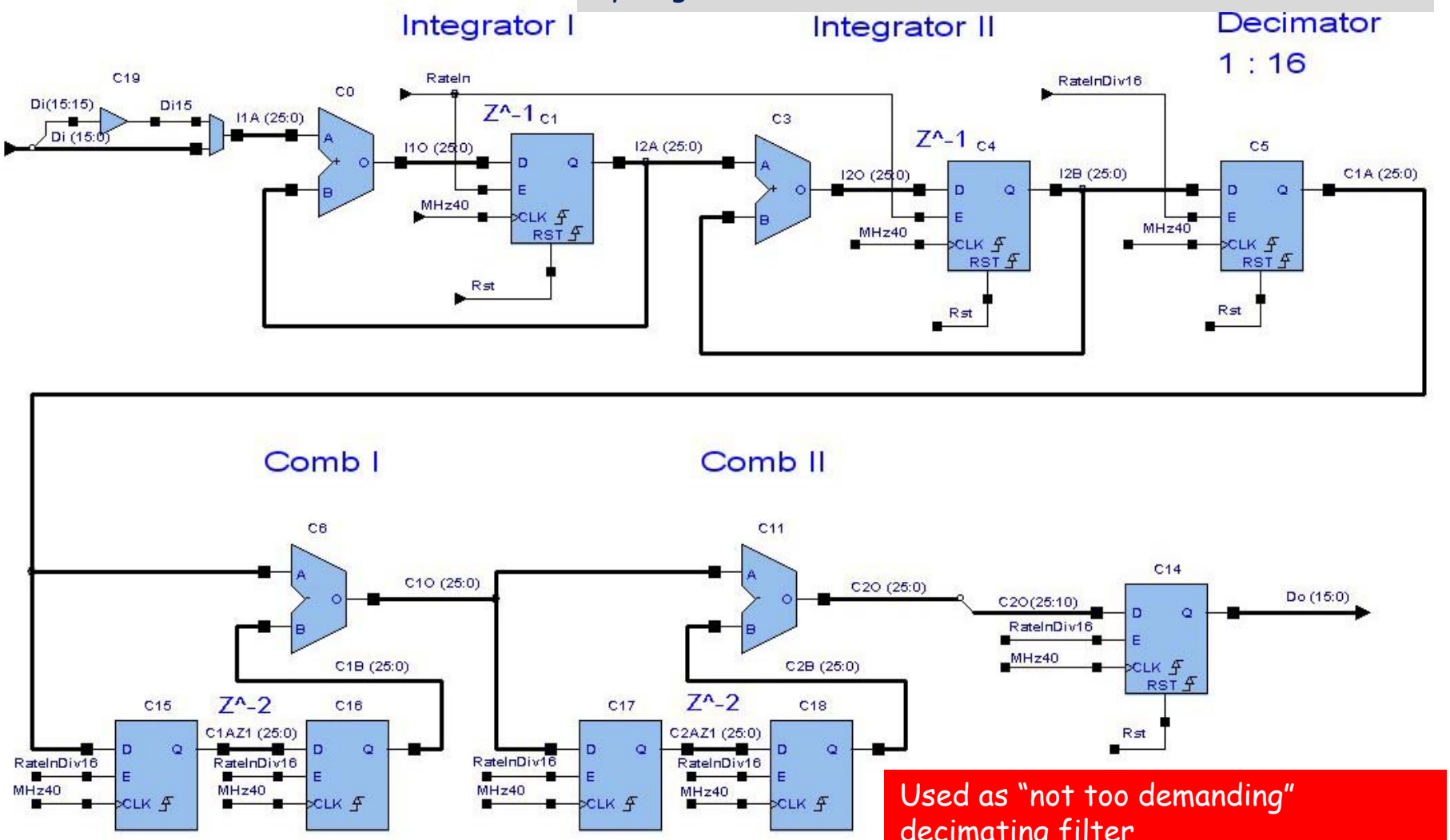
Courtesy of John Molendijk

Decimating filters

- The signals are sampled at 88.05 MHz. But in some application (tuning) the closed loop response is a few seconds only (mechanical part)
- Oversampling is good for Signal to Noise Ratio (SNR): The quantization noise of the ADC is (assumed to be) white noise extending from DC to the Sampling Frequency, and with a Standard Deviation of 1-2 Least Significant bits.
- After filtering, the noise power is reduced by the ratio filter BW/sampling frequency. Potentially a very significant improvement…
- But brute-force implementation of a few Hz LPF FIR clocked at 88.05 MHz will ask for a lot of resources (taps -> multipliers)
- The classic solution is Decimation: We Low-Pass filter the signal and reduce the sampling rate at the same time.
- Good fixed-point architectures are the Cascaded Integrator Comb (CIC) filter and the Half-Band filters

2 Stage CIC16

Cascaded Integrator-Comb filters. Classic decimating filter that uses accumulators only (no multiplier). Proposed by Hagenauer ~ 1985



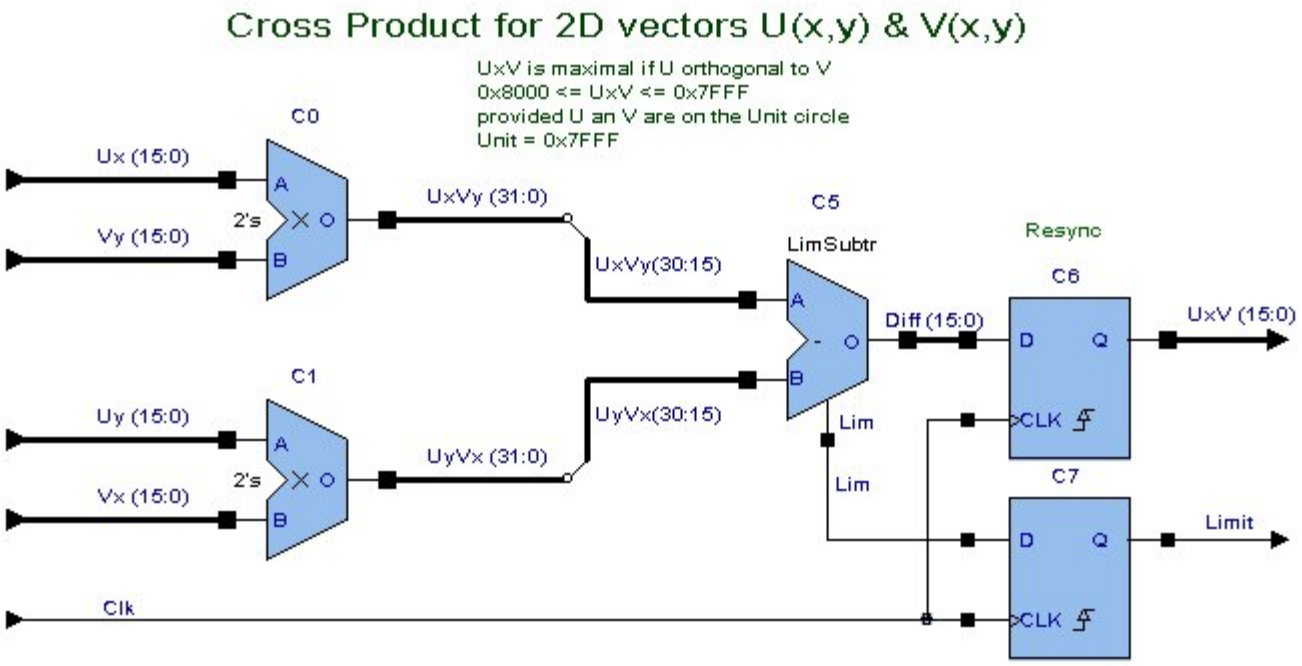
Used as "not too demanding" decimating filter

Courtesy of John Molendijk

Cross Product as Phase Discri

- $u \times v = u_x v_y - u_y v_x$
- $|u \times v| = |u| \times |v| \sin\theta = \varepsilon$ IcFwd
- u = Vacc, v = IcFwd

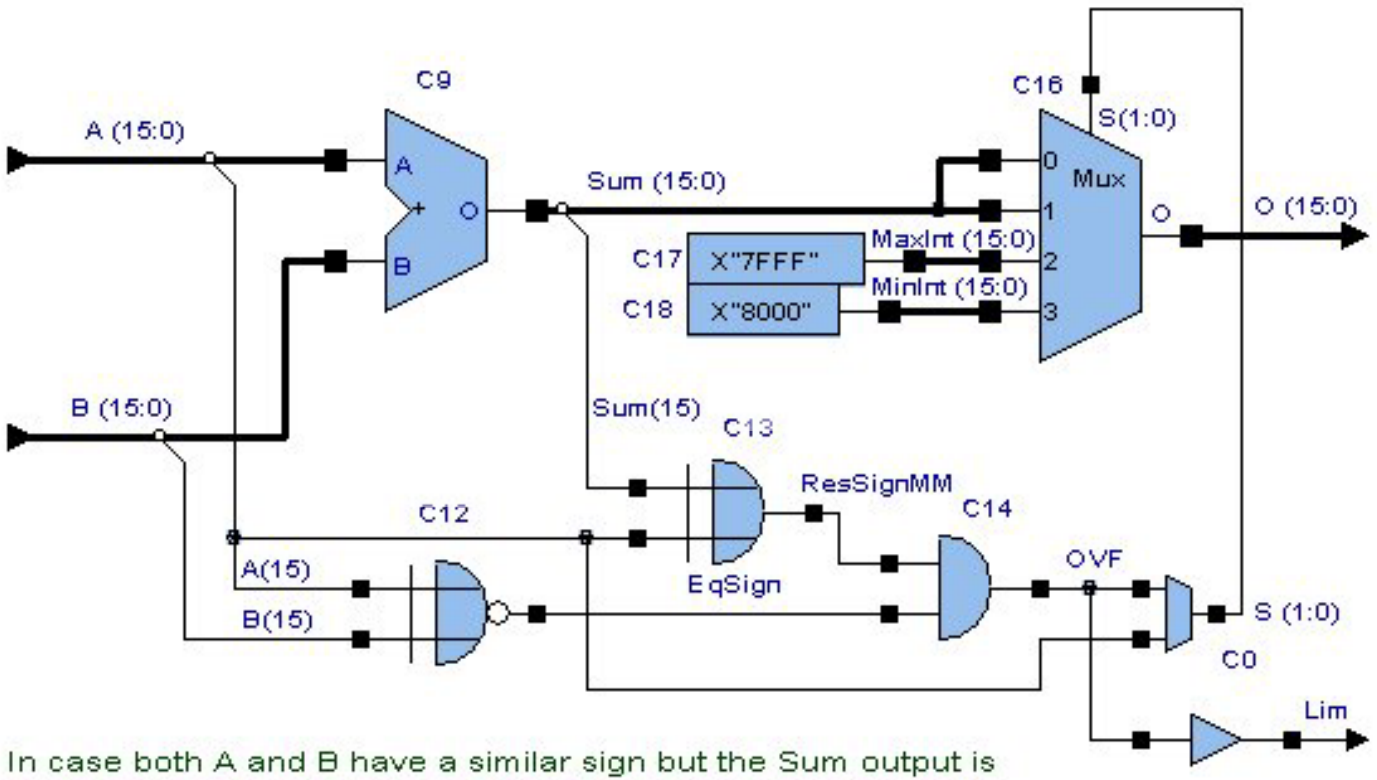
Used to measure phase shift Vcav-Icfwd for Tuning



Courtesy of John Molendijk

Limiting Adder

Very important: elegant saturation in case of adder output overflow



In case both A and B have a similar sign but the Sum output is of the other sign the output is set to be either MaxInt or MinInt depending on the input signal sign.

Courtesy of John Molendijk

Coordinate Rotation Digital Computer (CORDIC)

Imagine computing an Arctan[x] in fixed-point arithmetics….and with any desired precision…
No problem with the CORDIC….iterative algorithm…you set the number of digits…

- Iterative hardware algorithm for the computation of trigonometric functions
- Can also be used to compute square roots and divisions
- Uses shifts and adds only -> well suited for fixed-point FPGA implementation
- Pipe-lined implementation possible for higher throughput
- Proposed in late 1950s by J.Volder
- (To my knowledge) first use in an accelerator LLRF: RHIC (BNL) Beam Phase loop (M. Brennan, J. Delong, early 2000s)

- Consider a rotation by angle ϕ

$$x' = x\cos\phi - y\sin\phi = \cos\phi\left[x - y\tan\phi\right]$$
$$y' = x\sin\phi + y\cos\phi = \cos\phi\left[y + x\tan\phi\right]$$

- If the rotation angle is restricted to $+\!-\arctan[2^{-i}]$ the multiplication by the tangent term is reduced to a simple shift operation
- Arbitrary rotation can be achieved by a series of rotations of amplitudes $\arctan[1], \arctan[2^{-1}], \arctan[2^{-2}],\ldots$
- Let d_i be the decision whether to rotate in the positive or negative direction at iteration i (d_i=+-1) then the ith iteration can be written

$$x_{i+1} = K_i\left[x_i - y_i\, d_i\, 2^{-i}\right]$$
$$y_{i+1} = K_i\left[y_i + x_i\, d_i\, 2^{-i}\right]$$
$$K_i = \cos\left[\arctan\left(2^{-i}\right)\right] = \frac{1}{\sqrt{1+2^{-2i}}}$$
$$\text{with } d_i = \pm 1$$

- Let z_i be the rotation left to be done before iteration i we get

$$d_i = 1 \quad \text{if} \quad z_i \geq 0$$
$$d_i = -1 \quad \text{otherwise}$$
$$z_{i+1} = z_i - d_i \arctan\left[2^{-i}\right]$$

- The Rotation Form of CORDIC

- Example: rotation by 60.35 deg

i	Z (deg)	K	d	Arctan[2^{-i}] (deg)
0	60.35	0.707	1	45
1	15.35	0.894	1	26.56
2	-11.21	0.970	-1	14.03
3	2.82	0.992	1	7.12
4	-4.30	0.998	-1	3.57
5	-0.73	0.999	-1	1.79
6	1.06	0.999	1	0.89
7	0.17	1	1	0.45

Load the rotation angle in z_0

Iterate on i :

$d_i = 1 \quad \text{if} \quad z_i \geq 0$

$d_i = -1 \quad \text{otherwise}$

$$x_{i+1} = K_i \left[x_i - y_i \, d_i \, 2^{-i} \right]$$

$$y_{i+1} = K_i \left[y_i + x_i \, d_i \, 2^{-i} \right]$$

$$z_{i+1} = z_i - d_i \arctan\left[2^{-i}\right]$$

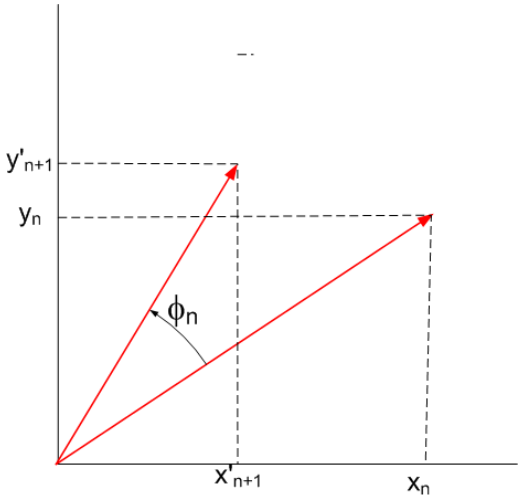
$$K_i = \cos\left[\arctan\left(2^{-i}\right)\right] = \frac{1}{\sqrt{1+2^{-2i}}}$$

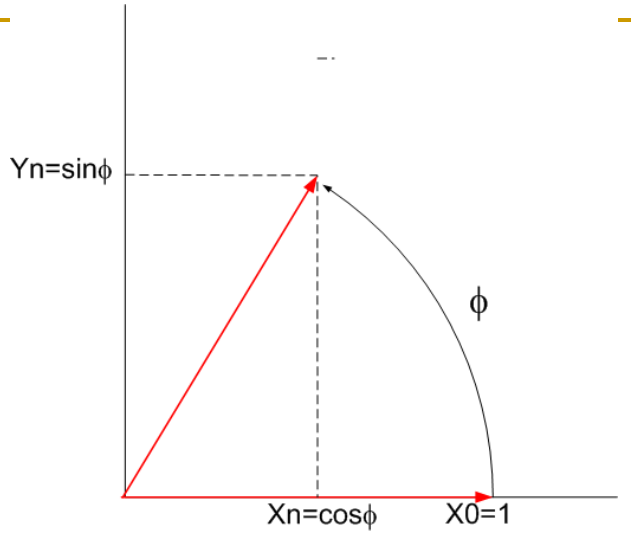
untill $z_n = 0$ or $n \geq \max\_nbr\_iterations$

- The values of *arctan[2^{-i}]* must be stored in a table
- The Rotation Form can be used to compute Cosine and Sine
- The Vectorial Form of the CORDIC starts with a vector (x,y) and compute its angle with respect to the x-axis.

Both forms are used in the Klystron Polar Loop

- The Rotation Form can be used to compute Cosine and Sine

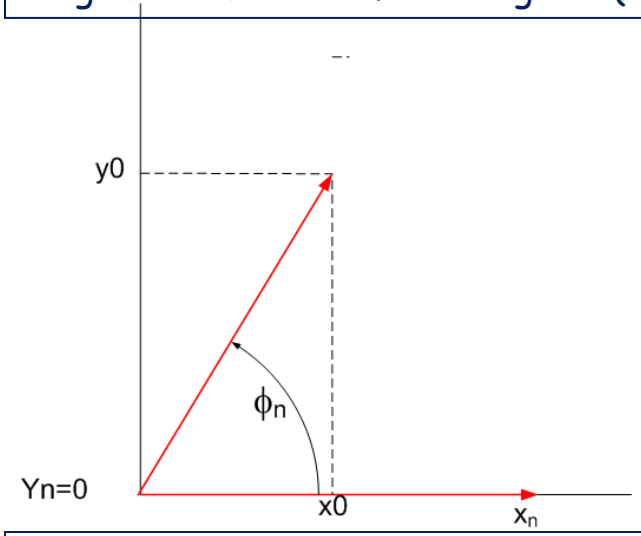




Rotation form with the original vector unit-length on the x-axis. Result gives (cosϕ,sinϕ)

- The Vectorial Form of the CORDIC starts with a vector (x,y) and keeps on applying the series of decreasing amplitude rotations untill the resulting vector is on x-axis (yn=0). It is used to compute magnitude and angle of a vector

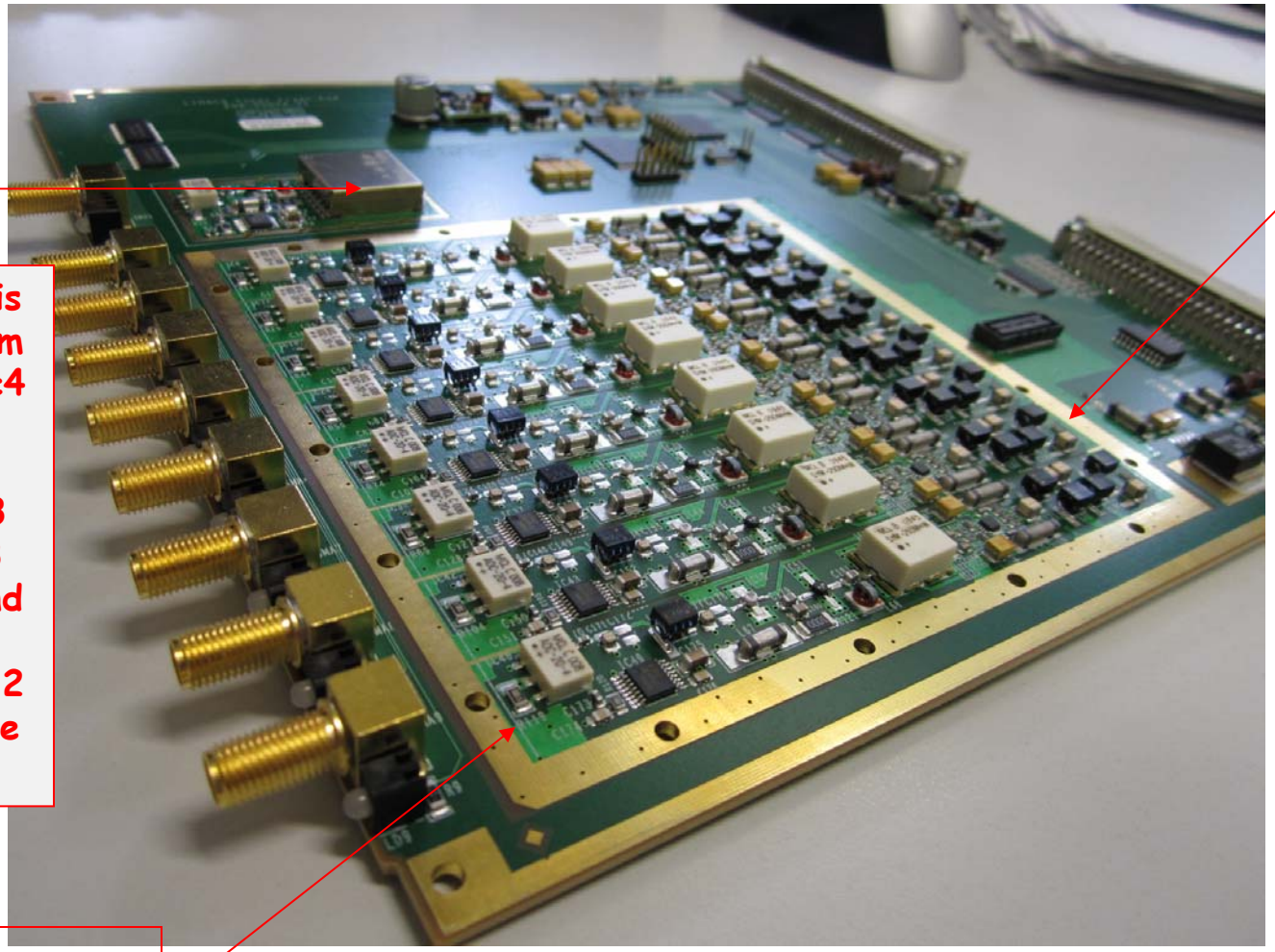
Both forms are used in the Klystron Polar Loop



Vectorial form:the original vector is rotated untill yn=0. The sum of the rotation angles gives the original ϕ (inverted)

PCBs

Tuner module: RF front-end



LO distri

8 channels is the maximum among Linac4 structures. It matches the DTL2-3 that have 3 antennas and 2 windows (2 fwd and 2 ref) plus one ref line

IF out (8 channels, differential)

RF demodulators (8 channels)

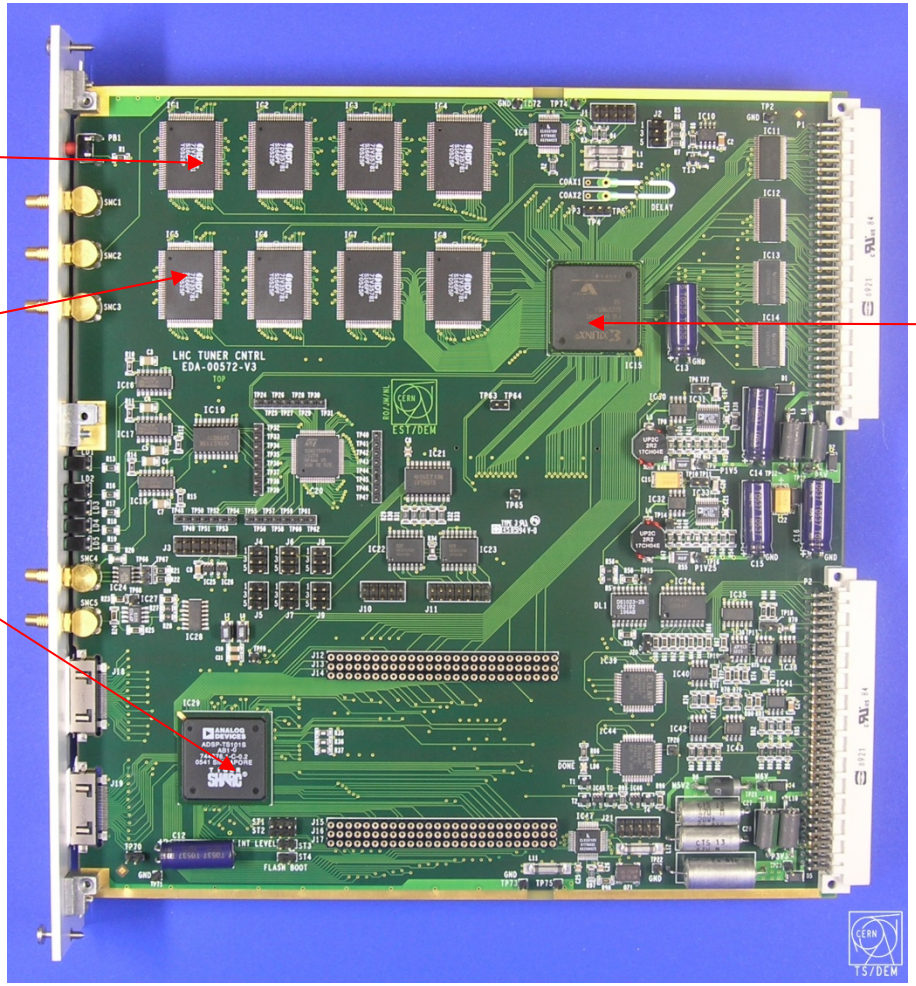
Linac4 Tuner module RF Front-end card. J. Noirjean

Tuner module: Processing card

Logging memory

Post-Mortem memory

Tiger Shark DSP. Slow Post-processing (floating-point)



FPGA
Fast Pre-Processing (fixed-point arithmetic), controls of the memories and VME interface

LHC Tuner module, processing card. J. Molendijk

If interested, contact John Molendijk or Jose Noirjean

Installation

LHC LLRF VME Chassis

Custom-designed VME crates used in the LHC and Linac4 (same crates)
VXI is also a popular standard (PEP2, SNS)

Thank you for your attention.

If you have liked it, join the LLRF club…Come to the next LLRF workshop in Autumn 2011

LLRF02
LLRF05 Cern
LLRF07 Knoxville
LLRF09 Tsukuba
LLRF11